

U R O P E A N E D I T I O N

EDN

THE DESIGN MAGAZINE OF THE ELECTRONICS INDUSTRY

NOVEMBER 10, 1994

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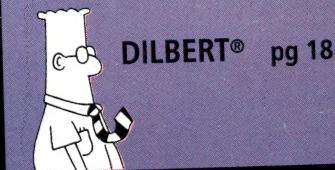
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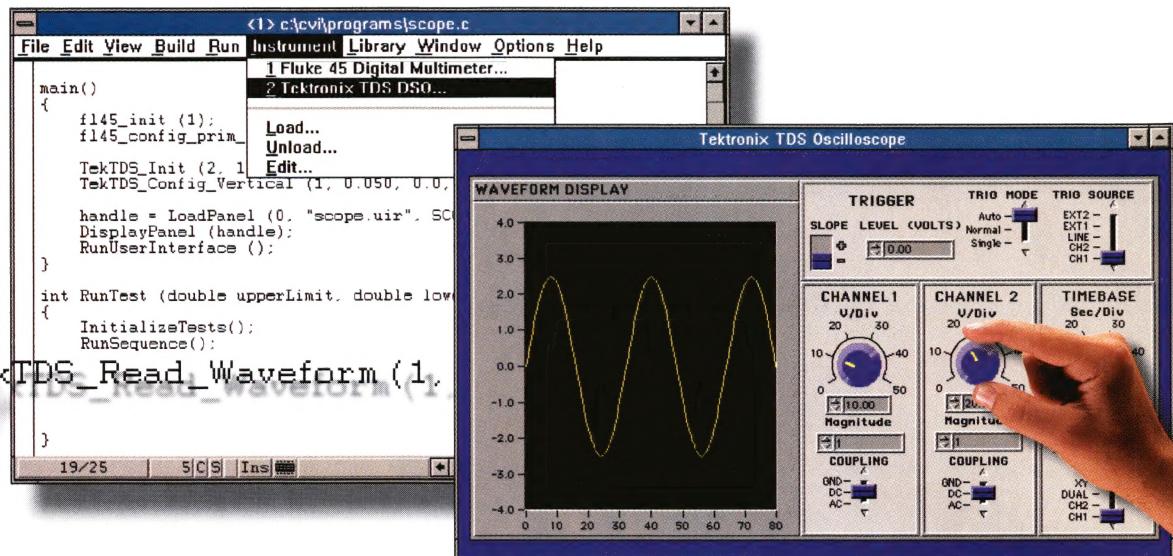


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and BIOS join to
green your PC pg 44**

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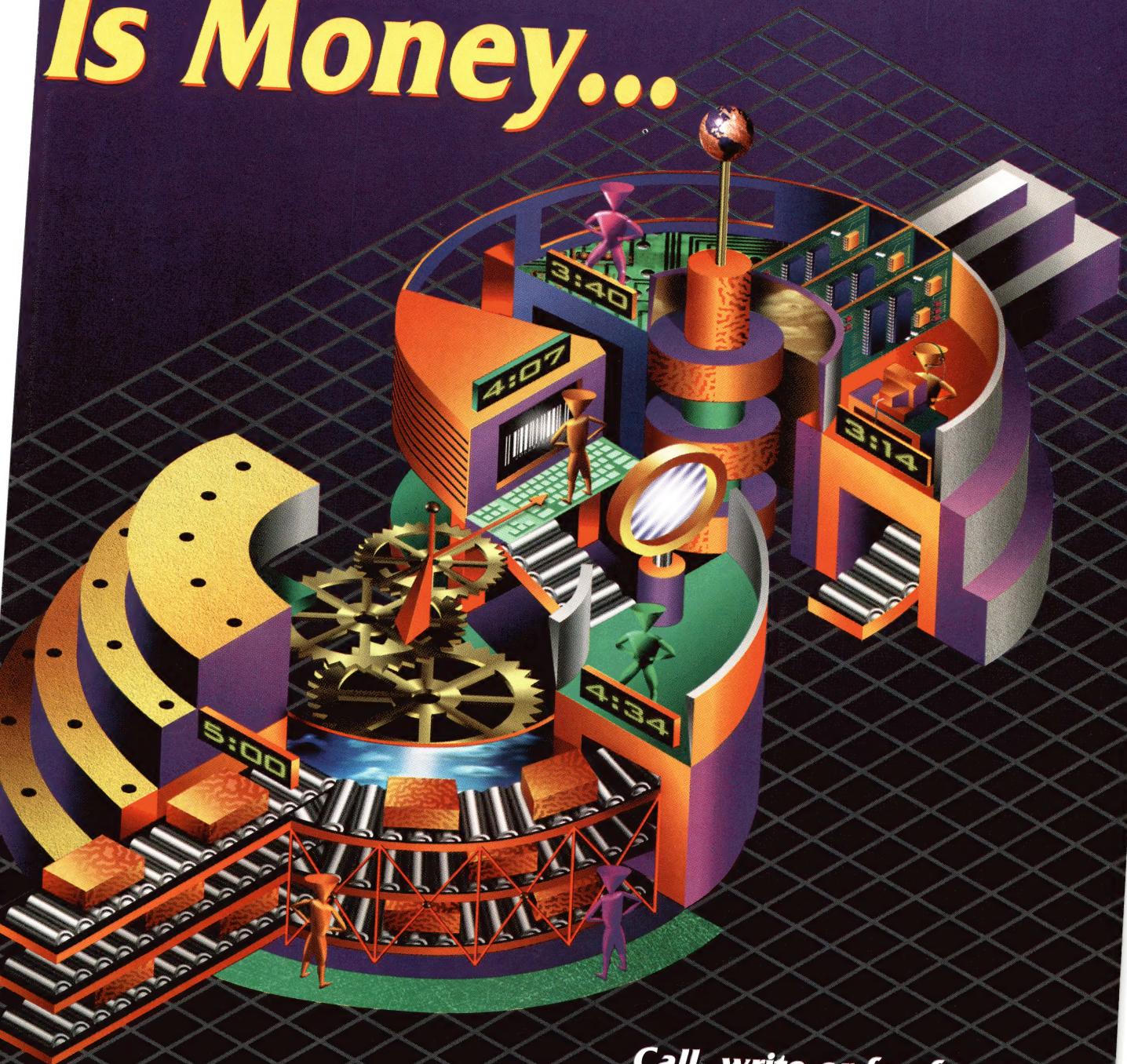


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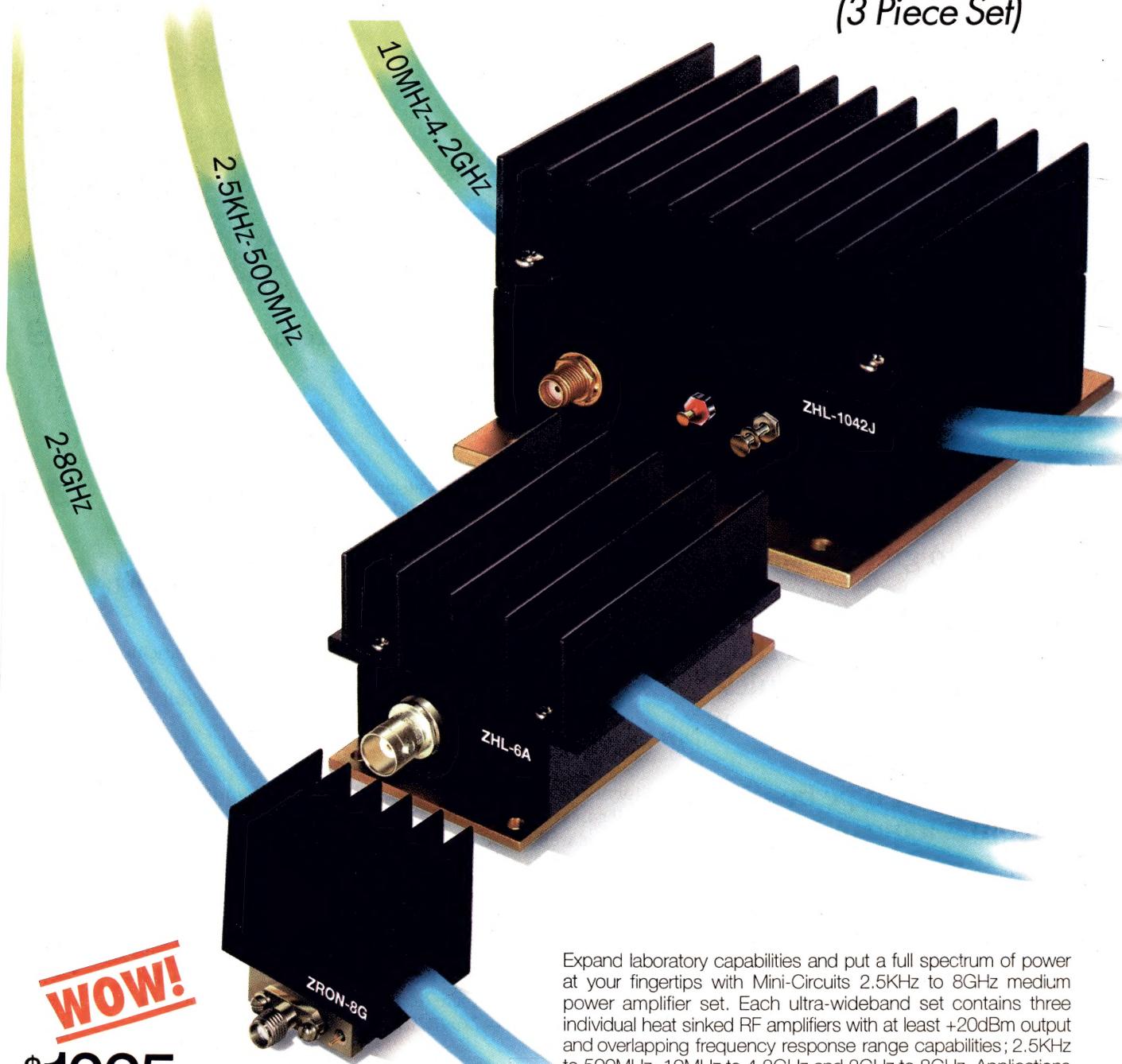
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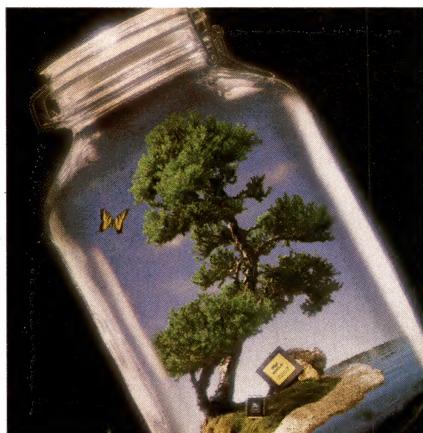
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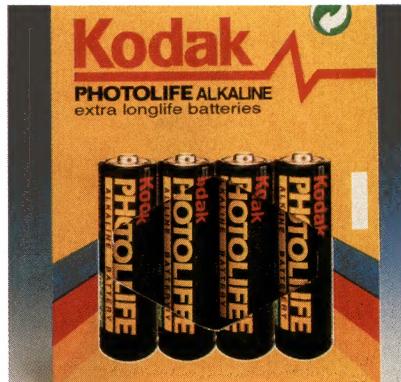


COVER STORY

GREEN YOUR PC

Cover photo courtesy Intel Corp; Digital photography by Richard Wahlstrom Photography Inc.

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Green Batteries

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EDN

CPUs, chip sets, and BIOS join to green your PC

DESIGN FEATURES

Green PCs, designed to better our environment through conservation, have become the norm. Although many peripheral devices have built-in mechanisms to manage power automatically, the majority of a system's green capability can be attributed to the CPU, its associated chip set, and the BIOS.—*Markus Levy, Technical Editor*

Green batteries: changing the rules for design

Getting green pc boards becomes a burning issue

Combine software tools to devise your own FPGA-verification environment

Green strategies cope with electronic products' energy and end of life

Secondary cache increases performance and reduces power use in portable PCs

Environmental concerns are changing much in our society—including the design of portable electronic products.

—*Dan Strassberg, Senior Technical Editor*

Constituents of today's pc-board material limit flammability but exude evil gases when burning. Tomorrow's pc-board material burns cleanly and is well ahead of controlling legislation.

—*Brian Kerridge, Senior Technical Editor*

Armed with working knowledge of a modeling language such as VHDL and a simulator, you can verify an FPGA's design and reduce prototype-debugging time. This article discusses verifying FPGA designs and provides concrete examples demonstrating this practical, low-cost approach.—*Leo Bredehoft, Netrix Telcom Systems*

Emerging design-for-environment techniques will help keep Mother Earth green.—*Jim Lippke, Consultant*

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135

For some time, the main focus of portable-computer development has been to extend the computer's operating time on a single battery charge. Performance considerations were secondary. However, now that portable operation ranges to eight hours plus, the focus is shifting toward improving operating performance. The new challenge is to improve operating speed without sacrificing the gains in mobile operation time.

—*J Thomas Pawlowski, Micron Semiconductor Inc*



Media accelerator blends audio, graphics, and video data **17**

Low-cost logic analyzer targets scope users **17**

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Digital tachometer avoids analog devices

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Dismantling a fuzzy rule-based system shows its inner workings

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—David Brubaker, *Fuzzy-logic Contributing Editor*

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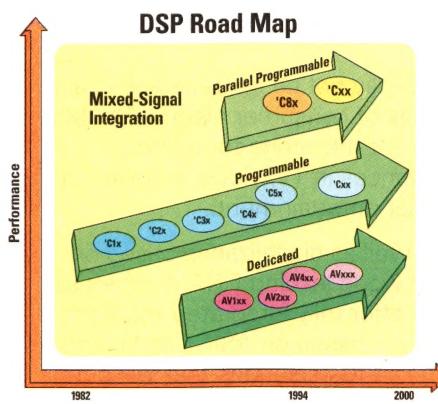
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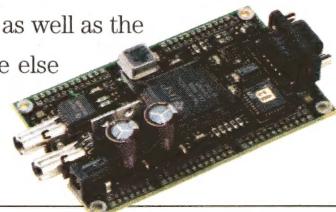
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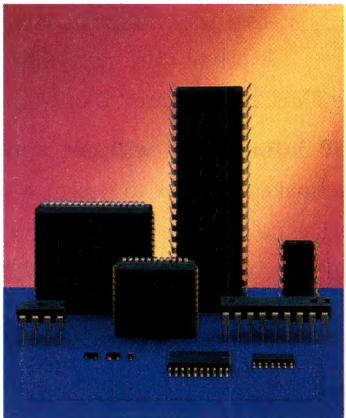
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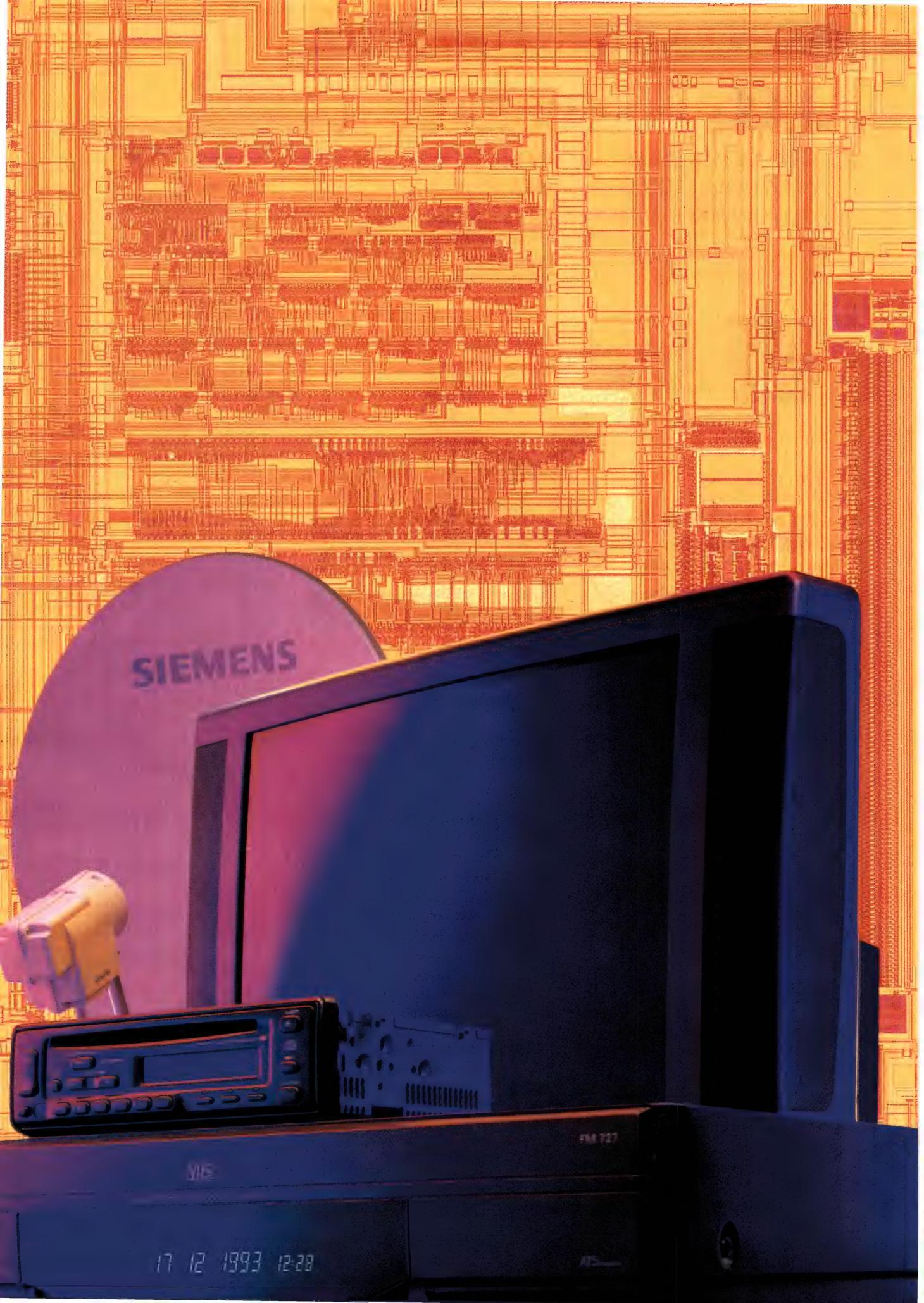
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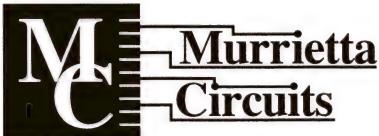


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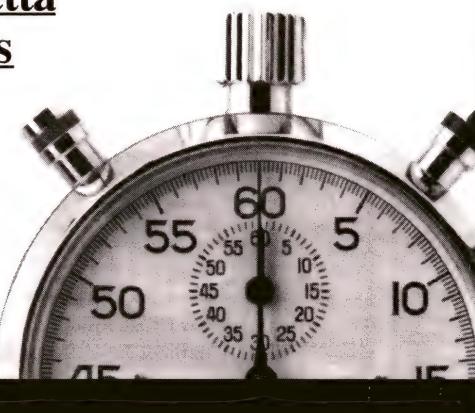
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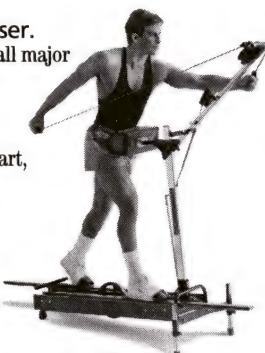
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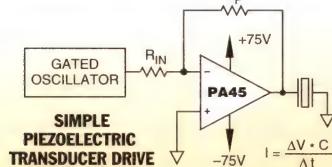
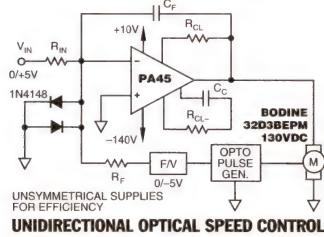
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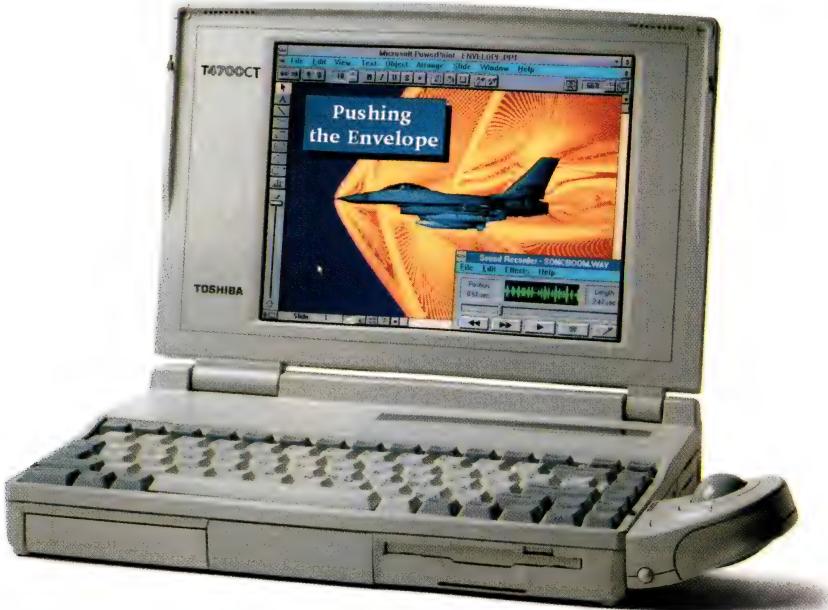
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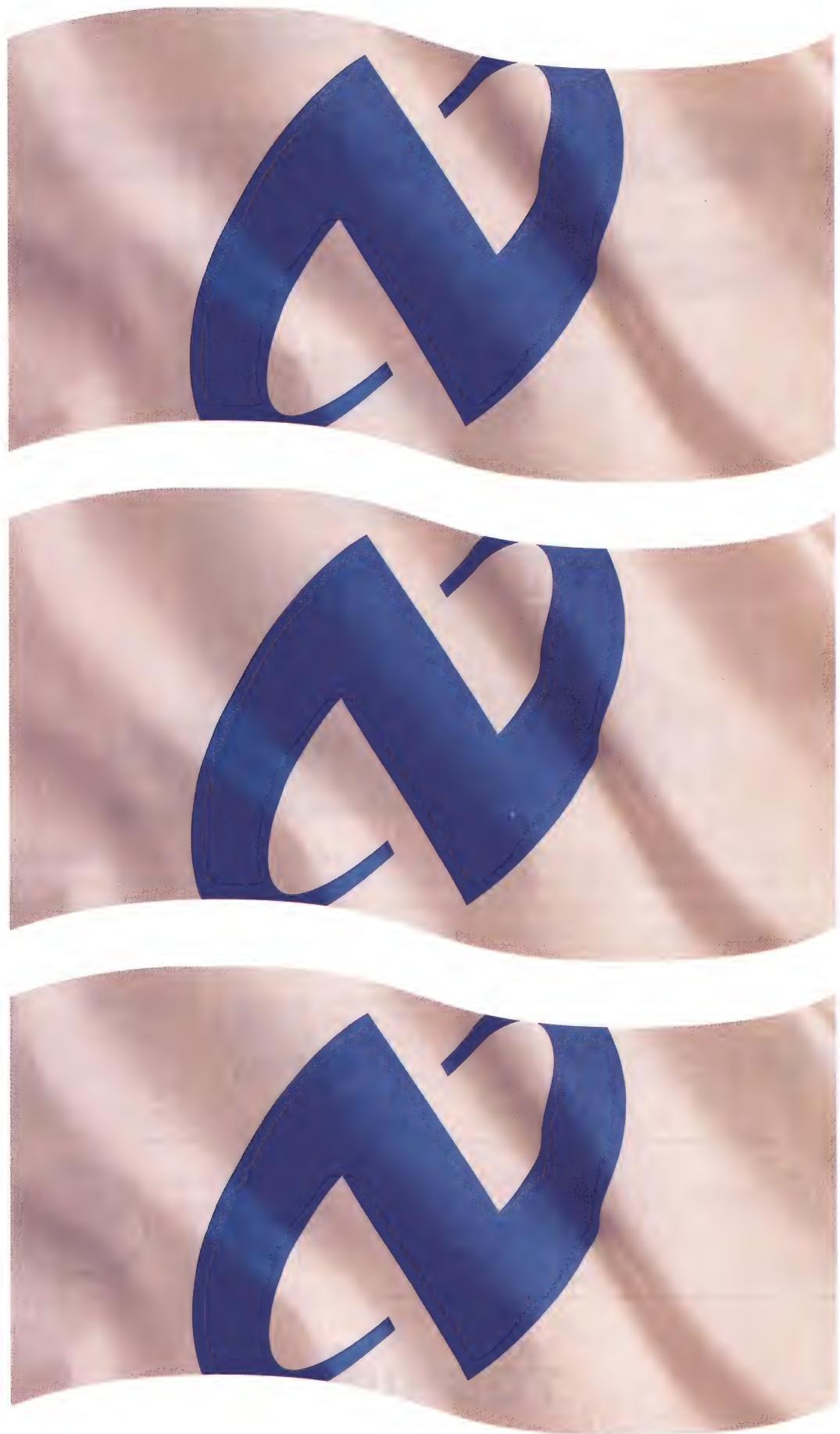
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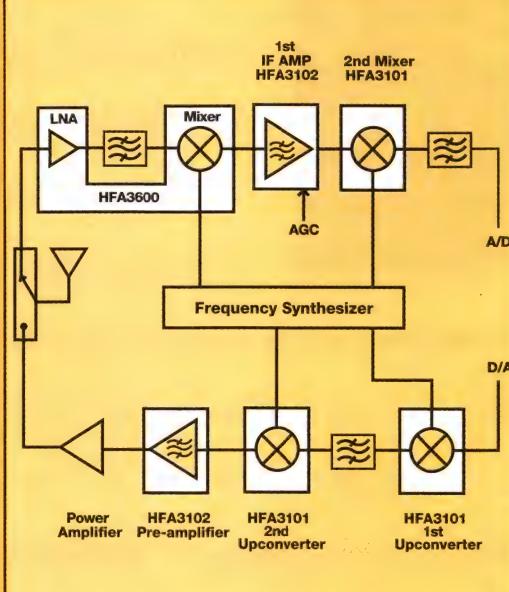


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Media accelerator blends audio, graphics, and video data

A new media accelerator from Brooktree provides high-performance graphics, 16-bit audio, full-screen 1280×1024-pixel graphics, and 30-frame/sec video windows in a single three-chip set. The product employs a packet-based multimedia architecture, a 1-Mbyte frame buffer, a suite of software drivers, and a connection to the PCI or VL bus. Brooktree is targeting the product for both add-in cards and the next generation of Pentium-based motherboards.

The BtV MediaStream includes software-based MPEG decompression and software-based wave-table synthesis. In addition, a BtV-based PC can optionally output all-digital sound directly to consumer devices with digital input ports, including digital audio tape and CD players. The MediaPacket architecture converts all multimedia data inputs, including sound, into data packets that a local bus transmits and processes.

The product comprises the BtV2115 MediaStream controller, an audio I/O-controller chip, and a packetized-data DAC (PACDAC) D/A converter that provides graphics and mixing capabilities. Because the PACDAC resides in the back end of the subsystem, video remains in its smallest native format until it passes through the MediaBuffer, a central unified buffer. This approach reduces memory, bandwidth, and quality problems below those of systems that scale up the video before sending it to the frame buffer.

The BtV2115 MediaStream controller provides graphics-user-interface acceleration (Blt, line, draw, pattern fill)

plus central video-in and audio-I/O control. An optional BtV VideoStream decoder allows video capture. In this mode, the BtV MediaStream subsystem handles all NTSC/PAL/S-video sources. Price for sample quantities of the chip set is \$95. Production quantities will be available in the second quarter of next year.—by John Gallant

Brooktree Corp, San Diego, CA, (800) 228-2777.

Circle No. 460



Brooktree's BtV MediaStream accelerates audio, graphics, and video in multimedia applications.

SPARC upgrade hits 90 MHz

A confluence of technologies allows **Ross Technology** to offer SPARC-system users upgrades that can replace 40- and 60-MHz CPUs with as many as four 90-MHz CPUs. The technologies include a three-layer-metal, 0.5-μm, 3.3V CMOS process from parent company Fujitsu, the HyperSPARC architecture, and a multi-die packaging technique using silicon substrates. Together, the technologies allow Ross to pack a CPU, a chip set, and a 256-kbyte cache into a 131-pin PGA, enabling SPARCstation M-bus modules to contain two CPUs each. The modules run at the bus-interface speed of the host system and provide their own 90-MHz clock for the CPU. SPARCstation 10 and 20 users and SPARCServer 630/70/90 users can use two modules, bringing as many as four CPUs into play. The upgrades range in price from \$5141 to \$17,870 and are SCD-compliant.—by Richard A Quinnell

Ross Technology Inc, Austin, TX, (800) 774-7677.

Circle No. 461

Low-cost logic analyzer targets scope users

One way to characterize HP's 54620A is to call it a \$2995, 16-channel logic-timing analyzer for people who have always done digital troubleshooting with a scope. Many people have found that learning to use a logic analyzer is simply too time-consuming. So they continue to use a scope, even though, once they became familiar with the logic analyzer, they could get the job done much faster.

HP bases the instrument's design on that of the highly successful 54600 family of low-cost digital storage oscilloscopes. After extensive market research, the designers stripped away some of the more arcane features of high-performance logic analyzers.

The result is a unit that—at its fastest sweep speed—takes 500M samples/sec (2-nsec resolution), captures 3.5-nsec glitches at any sweep speed, offers a delaying sweep and split-screen display like those familiar to most scope users, and includes a triggering system that is both flexible and easy to understand. The analyzer triggers on signal edges from any channel or an external source, high/low/don't-care patterns from all channels, logical combinations and sequences of patterns, and patterns that repeat for a specified number of times or a specified interval.

The analyzer's cursor- and automatic-measurement modes should be familiar to

(continued to pg 18)

scope users. Another feature helps you keep track of the meanings of the many displayed signals; a labeling facility lets you select signal names from a menu of standard names augmented by the 85 names you defined most recently. The unit groups its 8-pF-capacitance inputs into a pair of eight-channel pods.—by Dan Strassberg

Hewlett-Packard Co., Santa Clara, CA, (800) 452-4844.

Circle No. 462



Although HP's 54620A looks like a scope, it is a low-cost, 16-channel logic-timing analyzer with 2-nsec resolution and controls that users can learn rapidly.

Philips ties with IBM and buys HDL Systems

Philips Electronics and IBM are setting up joint manufacturing to increase Philips' capacity for 0.8- μ m wafers and to provide access to IBM's DRAM technology. The venture will be based at IBM's plant in Boeblingen Hulb in Germany, which manufactures 4-Mbit DRAMs. The companies are planning for Philips to

(continued on pg 20)

Processor-core deal adds vital element to ASIC range

An exclusive licensing agreement between Alcatel Mietec (Belgium) and Nordic VLSI (Norway) adds an 8-bit μ RISC processor core to other significant features of a new range of ASICs from Alcatel Mietec. Alcatel Mietec is one of Europe's leading suppliers of mixed-signal ASICs to automotive, industrial, and telecommunications markets. The new range—Intelligent Interfacing Technology (I²T)—aims to consolidate that position, ahead of closest rivals Motorola and Texas Instruments.

I²T ASICs use a 0.7- μ m, 5V CMOS process for high-density digital circuitry, to which you can add various modules to increase functionality, particularly for interfacing applications. The additions include Nordic's MTC-8308 μ RISC module, linear analog modules, high-voltage switching modules, and memory modules. I²T ASICs maintain compatibility with Mietec's ASIC device libraries, and the modular-design approach offers flexibility to control cost by limiting mask count.

Nordic's MTC-8308 core is a 40-MHz 8-bit processor with up to 4 kbytes of ROM, 192 bytes of RAM, and 31 instructions. Mietec has integrated a set of design tools that support Nordic's core into its "MADE" ASIC design system. The tools include a C compiler, a macro assembler, a VHDL model, a software simulator, and a hardware emulator.

I²T ASICs include 12V CMOS and bipolar modules (including an 18V capability for programming) for linear-analog functions. The ASICs also include 100V n- and p-type DMOS modules for high-voltage switching functions. By mid-1995, the company will add a one-time-programmable, nonvolatile, 100-bit memory module for functions such as identification and calibration. Other future additions include up to 8 kbytes of EEPROM, 64-kbit flash-memory modules, and 16-bit MTC-8316 and DSP MTC-8300 modules.

—by Brian Kerridge

Alcatel Mietec, Brussels, Belgium, 2 728 18 11.

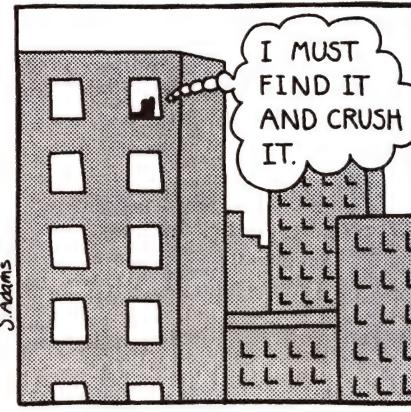
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license IBM's 16-Mbit technology for embedded DRAM applications in consumer and multimedia products.

Philips Semiconductors has also acquired 100% of HDL Systems (Sunnyvale, CA), a manufacturer of 32-bit μ Ps. Philips needs a 32-bit architecture to offer users a performance path from the 8-bit embedded 80C51 via the recently announced 16-bit 80C51 extension.

HDL's MR300 processor core—designed under Mips R3000 RISC license—provides Philips with an easily extensible architecture for the embedded-microcontroller market. The MR300 uses zero power when the clock stops; this static design is critical to Philips' many battery-powered applications.—by Brian Kerridge

IBM Europe, Germany, (7117) 853407.

Circle No. 465

Philips Semiconductors, Eindhoven, The Netherlands, (40) 722091.

Circle No. 466

Book helps you manage system power



As portable computers evolve, users are witnessing the trends toward

higher performance and longer battery life. Until now, battery life, alias power management, has been an art rather than a science. Even though the Advanced Power Management specification (from Microsoft, Intel, and Phoenix) defines a standardized interface between compliant applications and the system BIOS, many variables exist within each system's BIOS. For that reason, no one until now has attempted to write a book on the *science* of power management.

Now, James Bunnell has tackled the subject in his book, *Power Management That Works*, which formalizes and makes practical power-management concepts. Between the book's covers, Bunnell explains how to determine when a system is idle, the most

challenging aspect of the subject. Toward that end, he begins by breaking down the subsystems into simple and complex devices and discusses the mechanisms for monitoring them. The book also covers the user interface, suspending the computer, hardware and software interactions, and current and future power-management models. Bunnell doesn't believe in giving end users power-management options in their notebooks. (I agree: Figuring out how to use these options practically requires a three-day training course.)

The book is easy to read and comprehend and provides an extensive—perhaps excessive—use of analogies. Whether you're a system designer or just someone interested in the subject of PC power management, this book, at \$24.95, provides a lot of value.—by Markus Levy

Annabooks, San Diego, CA, (800) 462-1042. **Circle No. 469**

UK companies expand wafer-fab facilities

GEC Plessey Semiconductors (GPS), the only UK-owned CMOS manufacturer, will invest \$150 million in its Roborough, UK, CMOS ASIC plant. The investment will enable the company to move from 6- to 8-in. wafers and to quadruple output by 1996. GPS will devote around 10% of the investment to advanced process development, including 0.25- μ m geometry. The new facility will incorporate a clean-room-within-clean-room environment that reduces time to market, enhances wafer protection, and improves yield. The investment announcement scotches rumors that GPS might be sold to Rockwell.

In a second UK fab investment, NEC has selected Scotland in favor of California for an \$800 million investment in a new facility. The plant will output 0.35- μ m-process, 16- and 64-Mbit DRAMs and advanced ASICs at 20,000 8-in. wafers/month beginning in October 1996. The company chose to develop its NEC Semiconductors (UK) Ltd base due to high European demand and because the plant is NEC's most productive.—by Brian Kerridge

GEC Plessey Semiconductors, Swindon, UK, (793) 518128. **Circle No. 467**

NEC Semiconductors (UK) Ltd, London, UK, (71) 353 4383. **Circle No. 468**

Regulator lowers maximum dropout to 35 mV

According to Texas Instruments, low-dropout regulators (LDOs) have been a product waiting for a technology. The company now claims to have the technology, a linear BiCMOS process, and has introduced a family of LDOs, which, among other features, reduces dropout voltage by an order of magnitude compared with previous LDOs. At load currents of 100 mA, the maximum dropout voltages range from 35 mV (for the 4.85 and 5V output devices) to 60 mV (for the 3.3V output device). In addition, the regulators feature a typical quiescent current of 285 μ A (for inputs around 5V) that's independent of the load. Maximum sleep-state current is 1 μ A.

Most of the advantages of the TPS71xxQ family stem from using a PMOS device instead of the more traditional pnp pass transistor. Low dropout voltage results from the PMOS device's behavior as a low-value resistor. Regulator quiescent current is independent of the load because, unlike with pnp types whose base,

(continued on pg 22)

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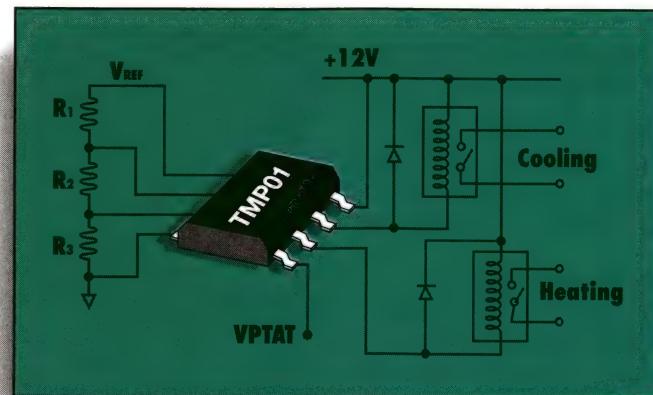


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The TMP01 is exceptionally easy to use. Upper and lower temperature limits and hysteresis are set by three exter-



nal resistors, with the exact set point values instantly calculated with accompanying design software. The sensor generates a voltage output proportional to temperature (VPTAT), with a sensitivity of 5mV/K over the temperature range.

Other TMP01 advantages include low power, single supply operation; 20mA open collector outputs to drive relays or to provide TTL/CMOS logic; over one month of continuous operation from a 9V battery; factory calibration to reduce manufacturing time and costs; and a variety of affordable plastic packaging options, starting at \$1.95.*

For more information on TMP01, contact your local Analog Devices sales office or representative listed below.



Analog Devices Europe: Austria (222) 88 55 04-0, Belgium (3) 2482619, Denmark (42) 84 58 00, France (1) 46744500, Germany 089/57005-0, 030/391 90 35, 04181/80 51, 0221/68 60 06, 0711/88 11 33, Israel (9) 911 415, Italy (2) 665 00 120, (11) 24 87 789, (6) 86 200 306, Netherlands (1620) 815 00, Sweden (8) 282 740, Switzerland (1) 820 01 02, (21) 803 25 50, United Kingdom 0932 266000

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CIRCLE NO. 4

output, and supply current are interdependent, a PMOS element is a voltage-driven device. Thus, operating currents are low and stable over the full load range, and specifications reflect actual loaded performance. Also unlike pnp-based LDOs, these regulators' supply current stays low even in dropout, whereas bipolar LDOs' supply current can increase and potentially cause start-up failures.

TI engineers concentrated not just on reducing dropout voltage and quiescent current but also on competitive noise and regulation specifications. These regulators have a 1% initial output tolerance and a maximum 2% tolerance over full line, load, and temperature ranges. Although you might not expect good noise performance from a low-power CMOS device, these regulators also compete with bipolar devices on this point. Typical output-noise spectral density at a 120-Hz frequency is $4 \mu\text{V}/\sqrt{\text{Hz}}$ for the 5V device.

In addition to the 5V (TPS7150), 4.85V (TPS7148), and 3.3V (TPS7133) versions, the family includes a 1.2 to 9.75V (TPS7101) adjustable regulator. Designed for 5V cellular systems, the TPS7148's 4.85V, $\pm 2\%$ output allows it to operate to the limit of 5V systems specified to $\pm 5\%$ tolerance, extending the operating life of the battery pack. Other features of these LDOs include a low-output-voltage indicator, sleep-mode shutdown, and operation with one small, external $4.7\text{-}\mu\text{F}$ tantalum capacitor. Package options include DIP, SOIC, and TSSOP. Prices range from \$1.45 to \$1.65 (1000).—by Anne Watson Swager

Texas Instruments, Literature Response Center, Denver, CO, (800) 477-8924, ext 3477.

Circle No. 470



The first products using Texas Instruments' linear BiCMOS process, the TPS71xx family of low-dropout regulators feature dropout voltages an order of magnitude lower than that of their purely bipolar counterparts.

Windows interprocess link runs 1000 times as fast as DDE

A new interprocess link proves a bonanza for developers of real-time applications that run under Windows. LT-Speedway not only offers performance 1000 times as fast as Windows' dynamic data-exchange (DDE) facility, but also lets you download the code free via the Internet. The code for the link is an Internet Anonymous FTP (file-transfer protocol) archive, which means that it's in the public domain. You need to "ftp" two files, LTSPEEDW.ZIP and LTP-SPEEDW.TAR.Z, from the /vendor/labtech directory at the ftp.uu.net site. Or get the same files from the Labtech forum library on CompuServe (type GO LABTECH).

To achieve its performance, LT-Speedway uses shared memory, thus avoiding Windows' single-threaded message queue. On a 90-MHz Pentium-based PC, the link transfers messages every 38 μsec . There is no limit to how much data a message can contain. The object-oriented software is not restricted to use with Windows applications; the link also runs under Harris Corp's Unix.

The software functions with object linking and embedding (OLE) V2.0 using OLE automation features. For Windows developers who require in-depth support, Labtech offers a \$1995 development kit that includes documentation, sample programs, and periodic code updates.—by Dan Strassberg

Labtech, Wilmington, MA, (508) 657-5400.

Circle No. 471

Test conference stresses high-level DFT, BIST, IDDQ

At this year's Silver Anniversary Edition of the International Test Conference, which took place in Washington, DC, from Oct 2 through 5, several trends appeared: The first is the emergence of tools for introducing test-related constraints into designs at the behavioral-modeling stage. Among companies offering such tools are LogicVision and Mentor. If these tools succeed, they will significantly reduce development time by eliminating much of the iteration IC design now requires.

The second trend is the growing recognition of the importance of built-in self-test (BIST) on ICs and the refinement of tools for synthesizing BIST structures—not just for RAM but for random logic. Examples of such tools come from AT&T Design Automation and IBM/Altium.

The third noteworthy trend is the increased level of discussion of IDDQ testing and the greatly increased number of commercial tools that support the technique. IDDQ detects faults in CMOS ICs

(continued on pg 24)

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V7040	R.G.B.		NTSC/PAL	Super impose function 75Ω drivers for: R.G.B. outputs and 2 composite video outputs	28P SDIP
CXA1228S		Y•color difference		Composite sync Sub carrier Line alternate outputs	28P SDIP
CXA1585Q	Decoder	Composite video	R.G.B.	Burst flag	32P QFP
CXA1950Q		R.G.B.	Y•color difference	Wideband chroma (2MHz) Sharpness filter	

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In fact, as a world leader in the design and manufacture of advanced semiconductors Sony offers much more than superior Encoders/Decoders. Its capacity for high volume production capacity allied to high level technical support is your guarantee of ultimate quality.

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Scandinavia, Italy & Other Areas: Tel: +44 256 478771 (Ext. 407).

Alternatively, write to Claire Dilly at:

Headquarters: Sony Semiconductor Europe, Priestley Road, Basingstoke, Hants RG24 9JP. Tel: +44 256 478771 (Ext. 431). Fax: +44 256 818194.

SONY®

CIRCLE NO. 203

by monitoring the supply currents, I_{DDQ} and I_{SSQ} . Many foundries have used I_{DDQ} for years as an adjunct to more widely known methods, but now its power and shortcomings are emerging. Among the companies showing I_{DDQ} products were AT&T Design Automation, Crosscheck, Cadence, Sunrise, Synopsys, and Teradyne.

Another trend evident at ITC focused on board test—now a mature industry. Although the number of systems that board-tester vendors ship continues to rise, system prices are declining even faster, so board-tester revenues are declining. Over the years, the emphasis in board test has gone from functional to in-circuit test and then to a combination of in-circuit and functional test. As surface-mount has become dominant in pc-board-assembly technology, the tester focus has shifted toward combining manufacturing-defects analysis (a simple form of in-cir-

cuit testing) and low-cost functional testing. Both Hewlett-Packard and Teradyne announced testers that add functional test to low-cost in-circuit test systems, and GenRad announced several low-cost application-specific functional test systems for boards and assemblies.

An area related to board test is boundary scan. LSI Logic reported that approximately 60% of new ASICs contain structures that enable board testing in accordance with the IEEE-1149.1 boundary-scan standard. Companies introducing new boundary-scan test products at ITC included Corelis and its European partner, JTAG Technologies, and Alpine Image Systems. These companies' products are low-cost test systems and test-system components. At the IC level, both National Semiconductor and Texas Instruments announced parts.

—by Dan Strassberg

Alpine Image Systems, Los Altos, CA, (415) 941-3247.
Circle No. 472

Altium, an IBM Company, San Jose, CA, (408) 534-4100.
Circle No. 473

AT&T Design Automation, Murray Hill, NJ, (908) 582-4083.
Circle No. 474

Cadence Design Systems Inc, Beaverton, OR, (503) 626-7117.
Circle No. 475

Corelis Inc, Cerritos, CA, (310) 926-6727.
Circle No. 476

Crosscheck Technology Inc, San Jose, CA, (408) 432-9200.
Circle No. 477

GenRad Inc, Concord, MA, (508) 369-4400.
Circle No. 478

Hewlett-Packard Co, Santa Clara, CA, (800) 452-4844.
Circle No. 479

JTAG Technologies BV, Eindhoven, the Netherlands, 31-40-782-584.
Circle No. 480

LogicVision, San Jose, CA, (408) 453-0146.
Circle No. 481

LSI Logic Corp, Milpitas, CA, (408) 433-8000.
Circle No. 482

Mentor Graphics Corp, Wilsonville, OR, (503) 685-7000.
Circle No. 483

National Semiconductor Corp, Santa Clara, CA, (800) 272-9959.
Circle No. 484

Sunrise Test Systems Inc, Santa Clara, CA, (408) 980-7600.
Circle No. 485

Synopsys Inc, Mountain View CA, (415) 962-5000.
Circle No. 486

Teradyne Inc, Agoura Hills, (818) 991-2900.
Circle No. 487

Teradyne, Boston, MA, (617) 422-3567.
Circle No. 488

Texas Instruments Inc, Dallas, TX, (214) 575-6396.
Circle No. 489

For information from all of the above companies circle just one number. **Circle No. 490**

Floppy-disk controller conforms to ISA Plug-and-Play standard

Standard Microsystems' FDC37C667 parallel-port Super I/O floppy-disk controller is the first such device to comply with the ISA Plug-and-Play standard (Version 1.0a). It also operates in systems running Microsoft Corp's soon-to-be-released Windows 95, known as "Chicago." Internal configuration registers allow you to program each of eight logical devices in the Super I/O chip. The eight logical devices are a floppy-

disk controller; two IDE interfaces supporting four drives, including a CD-ROM; a game port; a general-purpose address decoder; a multimode parallel port; and two NS16C550-compatible UARTs with 16-byte FIFO buffers for serial communications.

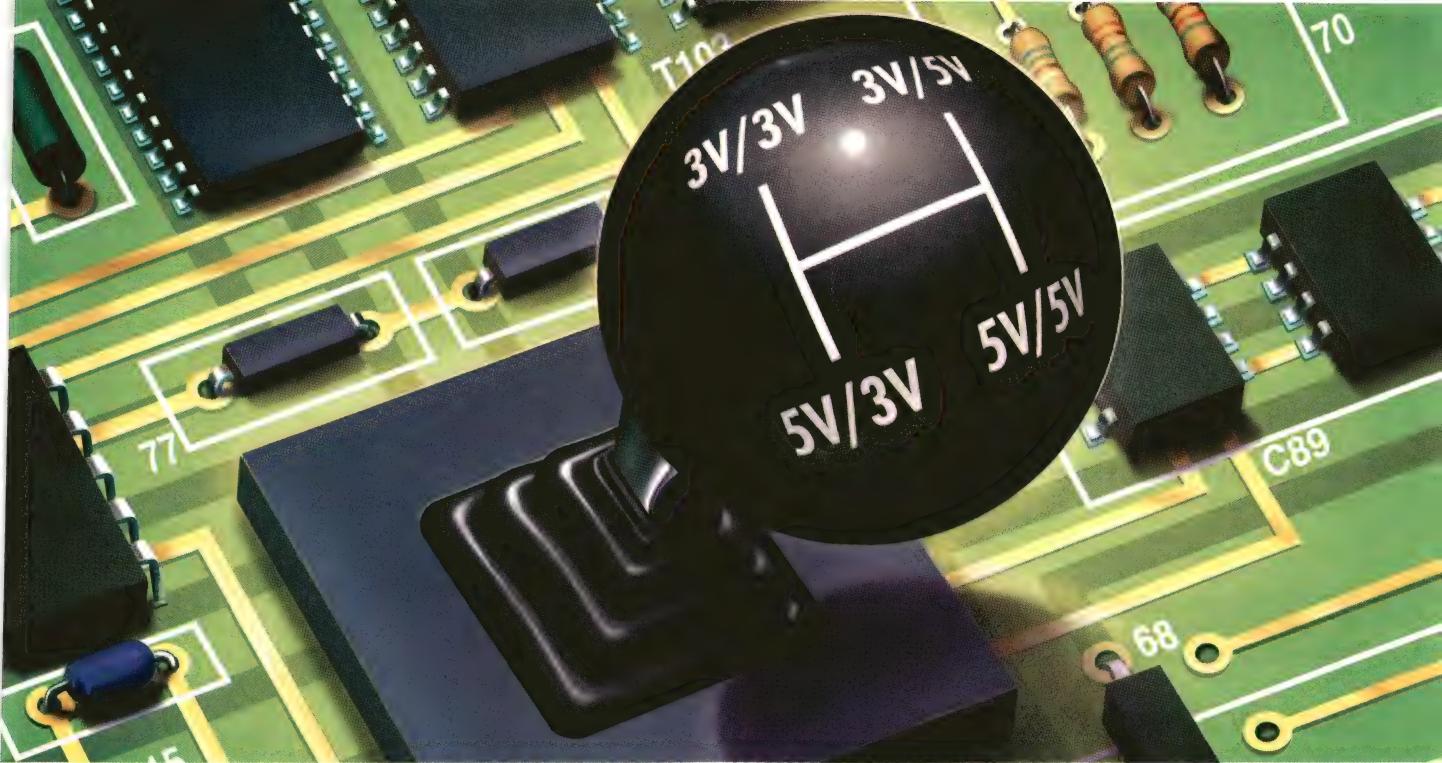
The multimode parallel port can operate in standard and enhanced high-speed modes and includes a ChiProtect feature that prevents damage to the chip during printer power-up. Operating in standard mode, the parallel port is compatible with ISA bus and PS/2 computer architectures. In high-speed mode, the port is compatible with the

enhanced parallel port (EPP 1.7 and EPP 1.9) standards and the extended-capabilities port (ECP) standard.

The chip comes in a 160-pin QFP and is configurable for motherboard or expansion-card applications. In motherboard applications, Plug-and-Play software allows the system to allocate resources using BIOS instructions. The chip has 15 selectable interrupt-request lines, three selectable 8-bit DMA channels, and three selectable 16-bit DMA channels.

An optional EEPROM interface allows nonvolatile storage of system configurations for use on reboot. In

(continued on pg 26)



POWER SHIFTER.

H4CPlus™ Series Gate Arrays let you select the voltage scheme that meets your power and performance goals.

Thanks to continually shrinking gate length and other process improvements, today's ASIC chips are able to run at lower voltages without giving up much performance—3V vs. 5V. However, the transition to complete 3V systems must wait until standards catch up and components are produced in economical volumes. So, it's become a mixed-voltage world in which designers are incorporating into most new designs both 3V and 5V components.

Single-chip solution to mixed-voltage challenges

Motorola's H4CPlus CMOS gate arrays are designed to interface between 3.3V and 5V, minimize power dissipation, and support high frequency communications, while cutting system cost. Now designers can choose the voltage scheme that provides the performance required at the lowest power.

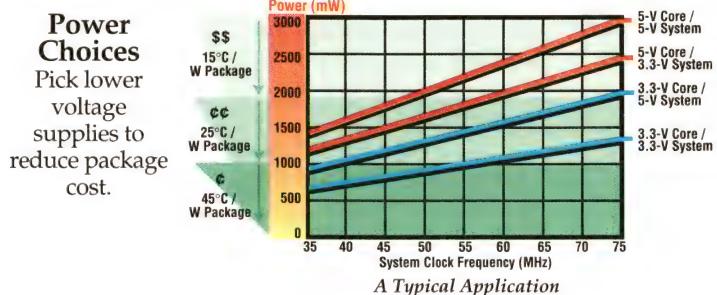
H4CPlus allows optimization of either the array core or I/O power—or both. Core may be 3.3V or 5V, I/O buffers 3.3V only, 5V only, or mixed.

H4CPlus Features

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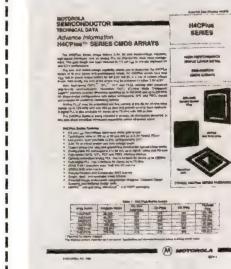
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Please send me H4CP/D data sheet.

647EDN111094



Name _____

Title _____

Company _____

Address _____

City _____

Country _____

adapter-card applications, an EEPROM stores the Plug-and-Play serial identifier, resource data, and a proprietary boot-configuration word.

The 0.8- μ m CMOS chip uses the company's SuperCell technology and incorporates an advanced digital data separator and CMOS 765B floppy-disk-controller core. The core supports data rates as fast as 1 Mbps for vertically recording floppy-disk and high-speed tape drives. The chip sells for \$10 (1000), and production orders ship 12 weeks ARO.—by John Gallant

Standard Microsystems Corp, Hauppauge, NY,
(516) 435-6000.

Circle No. 491

BOOK REVIEW

Survival in the EE shark tank

John A Hoschette's 200- μ g *Career Advancement and Survival for Engineers* proffers a variety of career-networking strategies and creative routes for improving your marketability as an EE.

Hoschette suggests proactive techniques for surviving corporate takeovers and downsizing, establishing and developing relationships with mentors, and exploiting the benefits of your company's continuing-education system. Hoschette, an electro-optics expert with 18 years of field-test, design-and-development, and management experience, derives much of the material in this book from a career-development course he cre-

ated with Honeywell in Minneapolis.

The text outlines 14 areas of career education and planning. "Are you in control of your career?" "Determining the formal and informal criteria by which you are judged," "What are the leading reasons engineers fail?" and "Getting on the fast track for advancement" are a sampling of chapter headings.

Hoschette's *Career Advancement and Survival for Engineers* costs \$39.95 (hardcover) and \$15.95 (paperback).

—by Jim Leonard

John Wiley & Sons Inc,
New York, NY, (800) 225-5945; (212) 850-6418.

Circle No. 492

EDA expert wanted

If you're an electronics engineer who knows electronic-design-automation (EDA) tools, *EDN* would like to know you. We're looking for a technical editor with the background and experience to interpret technical trends in EDA for our 160,000 readers. As an editor, you'll research, write, and edit articles; attend trade shows; and meet with industry leaders. We need someone who likes people, communicates well, and can balance several projects with fixed deadlines. Writing experience is desirable, but not essential. You can be based in Silicon Valley, the Pacific Northwest, or the Boston area. Our salaries are competitive with engineering positions. To discuss possibilities, call Gary Legg, Executive Editor, at (617) 558-4404 or send or fax your resume, salary requirements, and writing samples (if any) to Barbara Welensky, Human Resources Department, Cahners Publishing Co, 275 Washington St, Newton, MA 02158; fax (617) 558-4277. (An Equal Opportunity Employer, M/F/D/V).

Design kit speeds PCI-based ASIC designs

An electronic-design-automation tool kit for Synopsys' DesignWare product line makes it easier for designers to add a Peripheral Component Interconnect (PCI) interface to an ASIC. The kit includes a set of customizable high-level macros, a bus model for simulation, and a test suite to verify a design's compliance with the specification. The technology-independent macros include an interface, master and slave state machines, slave address recognizers and mappers, and master and slave data paths. The macros are fully synthesizable and allow you to use only those blocks you need for your implementation. A one-year license costs \$40,000. The macro set, bus model, and test suite individually cost \$30,000, \$23,000, and \$23,000, respectively.—by Richard A Quinnell

Synopsys Inc, Mountain View, CA, (415) 637-8212.

Circle No. 493

DC/DC converter meets Type I PCMCIA minimum thickness

In a 20-pin, 1.1-mm-thick TSSOP package, Linear Technology's LT1106 meets the maximum 3.3-mm thickness requirements for PCMCIA Type I flash-memory cards. With its 500-kHz switching frequency, the IC also allows the use of equally thin 10- μ H inductors and thin, low-value output capacitors. The flash-memory power-supply IC senses the available inputs from a PCMCIA connector and, if no 12V supply is available, generates 12V from either a 3.3 or 5V V_{CC} supply. To power 5V flash memories, the IC can also generate a 5V V_{PP} output from

V_{CC} . Thus, you can use the device to supply a 5 and 12V flash memories, guaranteeing a programming voltage even only a 3.3V supply is available at the PCMCIA connector. Other features include V_{PP} input-voltage-detection comparators, p-channel MOSFET control for V_{PP} -to-flash output switching, and shutdown to 9 μ A. The LT1106 (\$5.63) is available on tape-and-reel (2500-piece minimum order).

—by Anne Watson Swager
Linear Technology Corp, Milpitas, CA, (408) 432-1900.

Circle No. 494

SINGLE-DEVICE **5V TO 3.3V** POWER



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Now, from the innovator in integrated switching regulators, comes a new series of high-performance 5V to 3.3V, 3A and 8A single in-line products. The new Power Trends PT63/65 series lets you easily solve the problem of integrating 3.3V logic into existing 5V systems, *without redesigning your power supply.*

And, the PT63/65 family conserves board space with a profile as low as .36" x 2.00" x .60" (H).

Vertical, horizontal and surface mount versions are available.

The PT63/65 family features operating frequencies of 550KHz or more, 85% efficiency, over-temperature and short circuit protection. The PT63/65 family supports outputs of 2.1, 1.8, 1.5 and 1.2 volts.

If you're ready for a space-saving on-board power converter that you can plug right in, *call Power Trends for a sample today!*
1-800-531-5782.



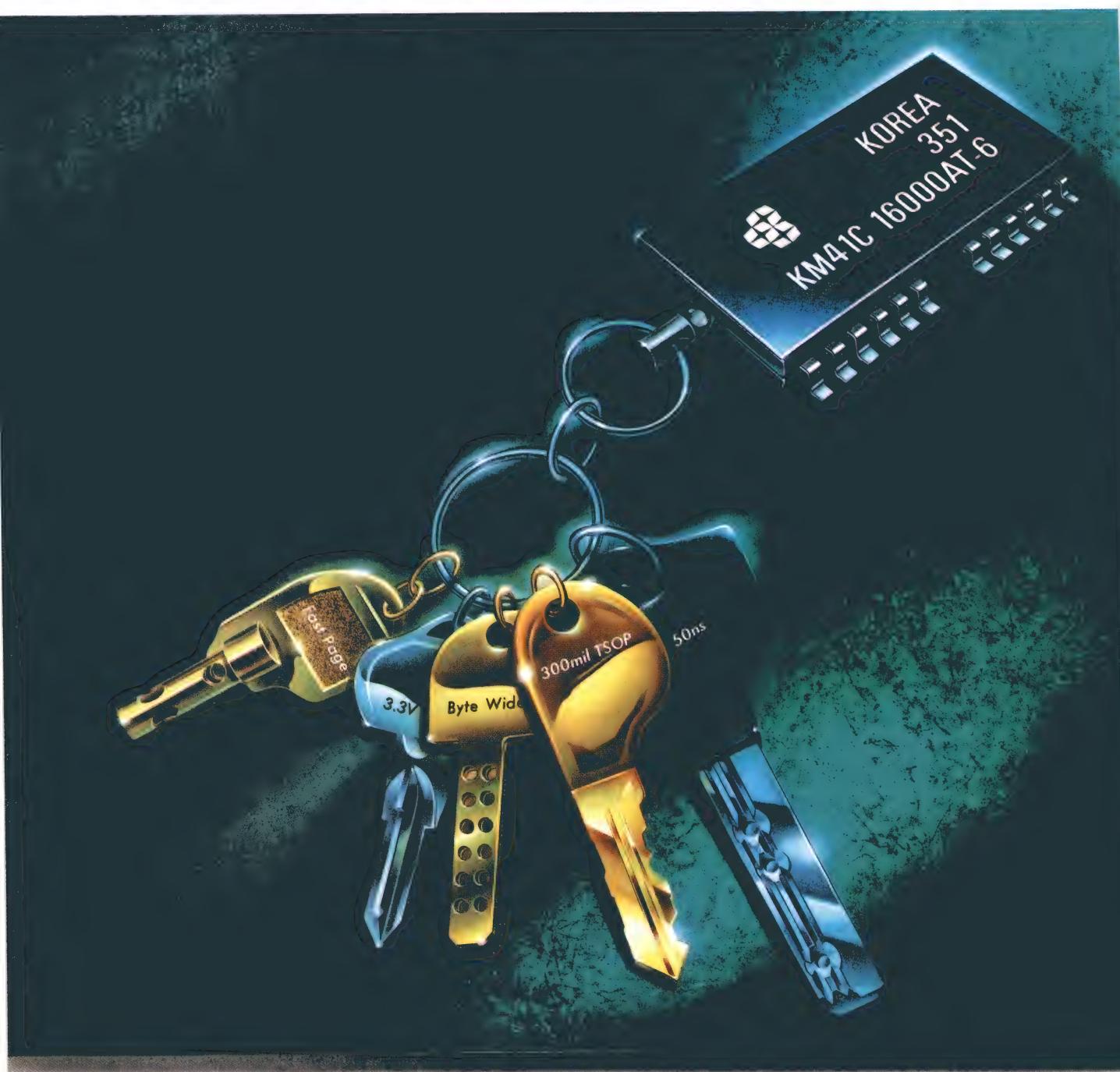
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CIRCLE NO. 66

EDN November 10, 1994 • 27

#1 16M DRAM PROVIDER... SAMSUNG



■ SEMICONDUCTOR BUSINESS

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What can you expect from Samsung, the company recognised around the globe for the technology that lead to the world's first dedicated 8-inch, 16M wafer production line?

Only the best...

Samsung stands ready to quickly respond to any customer needs with the finest quality products and services. These include a 16M DRAM, lead-on chip in a 300mil package — fully compatible with 4M DRAM package sizes — that is an exceptional choice for notebook PCs, high-end workstations, and everything in between.



Samsung's 16M DRAMs have been optimally designed in x1/x4 and x8/x16/x18 chip sets with fast access times of 50/60/70ns. A new extended data output(EDO) mode enhances access time over chips that use conventional fast page modes, with extreme energy efficiency drawing not 5volts, but a mere 3.3volts of power.

State-of-the-art DRAM technology from the leader, Samsung.

SAMSUNG

Organization	Mode	Part No.	Refresh
16MX 1	Fast Page	KM41C(V)16000A/AL/ASL/ALL	4096Cycle/64ms
4MX 4	Fast Page	KM44C(V)4000A/AL/ASL/ALL	4096Cycle/64ms
	Static Column	KM44C(V)4002A/AL/ASL/ALL	4096Cycle/64ms
	Quad-CAS	KM44C(V)4003A/AL/ASL/ALL	4096Cycle/64ms
	EDO (Hyper Page)	KM44C(V)4004A/AL/ASL/ALL	4096Cycle/64ms
2MX 8	Fast Page	KM48C(V)200A/AL/ASL/ALL	4096Cycle/64ms
		KM48C(V)2100A/AL/ASL/ALL	2048Cycle/32ms
1MX16	Fast Page	KM416C(V)1000/L/LL	4096Cycle/64ms
		KM416C(V)1200/L/LL	1024Cycle/16ms
1MX 4	Fast Page	KM44C(V)1000C/CL/CSL/CLL	1024Cycle/16ms
	Static Column	KM44C(V)1000C/CL/CSL/CLL	1024Cycle/16ms
	Quad-CAS	KM44C(V)1003C/CL/CSL/CLL	1024Cycle/16ms
	EDO (Hyper Page)	KM44C(V)1004C/CL/CSL/CLL	1024Cycle/16ms
4MX 1	Fast Page	KM41C(V)4000C/CL/CSL/CLL	1024Cycle/16ms
	Static Column	KM41C(V)4000C/CL/CSL/CLL	1024Cycle/16ms
	EDO (Hyper Page)	KM41C(V)4004C/CL/CSL/CLL	1024Cycle/16ms

* 'V' in Part No. means 3.3V part

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ELECTRONIC DEVICE GROUP

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Low voltage operation and energy savings are the two most critical factors driving next-generation portable and "green" electronic product designs. That's where Mitsubishi's extensive line of low-voltage ICs and high-efficiency RF devices can help you reduce power consumption and increase performance.

Mitsubishi 3V ICs can help reduce system power by as much as 50%, significantly extending the battery life of portables. Plus, low-power ICs enable increased system performance while still drawing less power than at 5V. Mitsubishi's extended temperature range

PRODUCT	DENSITY	V _{CC}	I _{CC} (Typ.)	I _{Sb} (Typ.)	FEATURES/BENEFITS
Synch. Cache DRAMs	16M, 4M (x4, x16)	3.3V	170mA	5mA	LVTTL Compatible; Burst & Power Down Modes; Ext. Ref.
Synchronous DRAMs	16M (x4, x8)	3.3V	180mA	2.5mA	Burst & Power Down Modes
EDO DRAMs	16M, 4M	3.3V	120µA	1mA	Hyper-page Mode; Ext. Ref.; Low SER
DRAMs	16M/4M	3.3V	75mA/60mA	500µA/120µA	Reduced Switching Noise; Low SER; Self Refresh
Flash ICs	1M (x8)	5.0V (V _{pp} =12.0V)	15mA	50µA	Bulk Array; Power Up/Down Data Protection; Ind. Temp.; Volume Capacity
Flash ICs	1M (x16)	5.0V (V _{pp} =12.0V)	25mA	50µA	Worldwide Architecture; Socket Compatible with x16 EPROMs/OTP ROMs
Flash ICs	4M (x8, x16)*	5.0V (V _{pp} =12.0V)	35mA	50µA	32 Blocks (16KB/8K word); Optimized for Data Storage; Auto Program/Erase
Flash ICs	16M (x8)	3.3V (V _{pp} =12.0V)	15mA	0.5µA	Easy Upgrade from Ind. Std. 8MB Flash Designs; Auto Program/Erase; Deep Power Down Mode; 32 Blocks (64KB ea.)
IC Cards	256KB-40MB	3.3/5.0V	110mA	150µA	Ext. Configurable; 1.4µA Data Ret.; Type I PCMCIA/3.3mm
I/O Cards (10 Base T)	-	5.0V	250mA	-	LAN; Ext. Configurable; Type II PCMCIA/5.0mm
I/O Cards (24/96)	-	5.0V	150mA	-	Fax/Modem; Ext. Configurable; Type II PCMCIA/5.0mm
Low Power Slow SRAMs	4M (x8)	3.3V	25mA	.4µA	Low Standby Current; Ext. Temp.; TFT Cell
Low Power Slow SRAMs	1M (x8, x16)	3.3V	8mA/15mA	.05µA/1µA	Low Standby Current; Ext. Temp.; TFT Cell
Fast SRAMs	256KB (x8)	3.3V	100mA	100µA	High Performance; Low Power; Ext. Temp.
Fast SRAMs	1M (x1, x4)*	3.3V	100mA	100µA	High Performance; Low Power; Ext. Temp.
Fast SRAMs	1M (x8)	3.3V	100mA	100µA	High Performance; Low Power; Ext. Temp.

*User Selectable

PRODUCT	V _{CC}	I _{CC}	FEATURES/BENEFITS
Baseband ICs	3.3V	16mA (max.)	On-board Scrambler, Comander, Modem
Battery Recharger ICs	3.0/5.0V	18mA/15mA (typ.)	On-chip D/A Converter; Maximizes Battery Life
D/A Converters	3.0V	3.5mA (max.)	8-bit; 12- and 36-channels
DC-DC Converter	2.5V	1.3mA (typ.)	For Backlight Control; Output Short Protection; High Speed Switching (300kHz)
LCD Controller Driver	5.0V	-	Low Power, Dot Matrix LCD Control
Dual PLLs	1.8V	7.5mA (typ.)	410MHz; Various Power Save Modes
Reset ICs	2.5V	1mA (typ.)	Reduces MCU Power Diss; Low Power 2-output; Memory Backup Avail.
GaAs MMICs	3.4V	250mA	800MHz-1.9GHz Band Operation; 60% eff.; Leadless Pkgs.
0.8µm Gate Arrays/ECAs	3.0V*	-	Very Low Power Diss.; 0.8µW/MHz/gate @ 3.0V; up to 400K Gates
8-Bit LCD MCUs	2.7V	1.6mA (typ.)	Up to 48KB ROM On-chip, LCD Controller
8-Bit Keyboard MCU	2.7V	1.6mA (typ.)	Keyboard Controller, Host Interface
8-Bit MCUs with Custom Logic Functions	2.7V	1.6mA (typ.)	3.0V up to 20MHz clock; User-defined Functions
8-Bit Magicbus® MCUs	2.7V	1.6mA (typ.)	Up to 32KB ROM
16-Bit High Performance MCUs	2.7V	4mA (typ.)	Up to 60KB ROM/2KB RAM or ROM-less; High On-chip Integration

*Fully Characterized for 3.0V

the company has eliminated CFCs, including 1,1,1-trichloroethane solvent and carbon tetrachloride, in manufacturing processes at all its semiconductor production facilities. The company is committed to reducing industrial wastes by 30% in 1995, cutting energy consumed in semiconductor production processes by 25% by the year 2000, and is conducting R&D in recyclable packaging, as well as in solar power energy sources.

For more information on Mitsubishi components for portable and "green" designs, or for details on environmental policies and activities, call **1-800-785-0004, Ext. A** or 408-730-5900, Ext. 2106.



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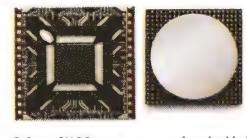
MMICs up to 60% efficiency



Battery Recharger ICs maximize battery life



3.3V CDRAMs, DRAMs & SDRAMs with enhanced power management for "green" projects



0.8µm CMOS gate arrays and embedded cell arrays, up to 400,000 gates



Mitsubishi Electric's
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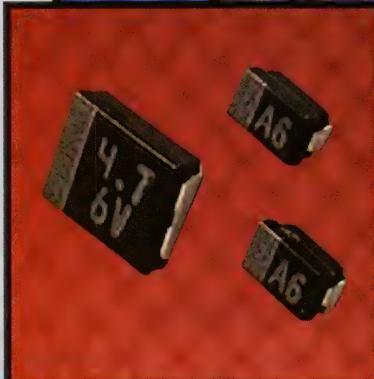
GaAs MMICs offer 60% efficiency helping cut power requirements and increase durability in wireless portable products.

For "green" PCs, monitors and printers, Mitsubishi 3V ICs help designers meet the U.S. Environmental Protection Agency's (EPA) Energy Star™ Program requirements

to reduce standby system energy consumption to $\leq 30W$, conserve energy, extend equipment life and reduce environmental pollution.

In addition to creating enabling components for portable and "green" end-product designs, Mitsubishi Electric Corporation is committed to "sustainable development." To this end,





Everyone wants their surface mount capacitor supplier to have ISO 9000 certification. That's why we've certified all of our manufacturing facilities. Not just one or two.

And nobody gives you a wider or more reliable choice of surface mount aluminum electrolytic and tantalum chip capacitors than Nichicon.

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Reader notes correct source

While reading "Canny choices condense CPLD and FPGA design cycles" by Sung C Hu (EDN, August 4, 1994, pg 91), I found a mistake in the attribution of the quote "There are three kinds of lies: lies, damned lies, and statistics." Its origin actually lies with British Prime Minister Benjamin Disraeli, not Mark Twain.

*Tom Nath, Senior Engineer
Thomson Consumer Electronics
Indianapolis, IN*

Be wary of VHDL bandwagon

Although I enjoyed reading "VHDL emerges as a commercial design tool" by Karen Bartleson (EDN, August 18, 1994, pg 84) and share her enthusiasm for hardware-description languages, I strongly advise design and CAD engineers to consider Verilog HDL before blindly rushing to adopt VHDL. Verilog's syntactical kinship to C permits designers to learn it quickly and to write terse, readable, accurate code efficiently and cost-effectively. The Verilog equivalent of Bartleson's 16-bit VHDL counter model would be half as long and far more reader-friendly.

Before investing money and time to learn VHDL, the C-literate design engineer should try a free taste of Verilog by downloading the student version of the VeriWell/386 simulator from Well-spring Solutions (Sutton, MA).

*John A Eldon
Principal Systems Engineer
Raytheon Semiconductor
San Diego, CA*

Defense conversion troubling in real-world economy

I'm delighted to see EDN tackling the issue of defense conversion (Project Plowshare: Putting military technology to other uses, EDN, August 18, 1994). And it's high time—after five plus years of layoffs. I think, however, you miss an opportunity to address the concerns of your readers who have spent their entire careers in defense contracting.

I'd like to know how many of the EEs

who worked on NAVSTAR, for example, are now employed at GPS-based companies. And it might be useful to look at commercial companies' abiding prejudice against job applicants with experience on DoD projects. Even in industries such as medical electronics, where ruggedizing and high reliability are important, most managers see no crossover of skills.

Retraining efforts thus far (like the attempt to turn a handful of Southern California EEs into environmental engineers) have been feeble at best. This issue needs to be addressed before the industry loses more mature engineering talent.

*Kate Colborn, Editor
Diversity/Careers in Engineering
Center Harbor, NH*

Add another vendor

The following supplier of design-for-test tools was omitted from the list of vendors on pg 28 in "ASIC Test: It's a new ball game" (EDN, September 29, 1994):

LogicVision
San Jose, CA
(408) 453-0146

Circle No. 366

Subtleties and suggestions for power distribution

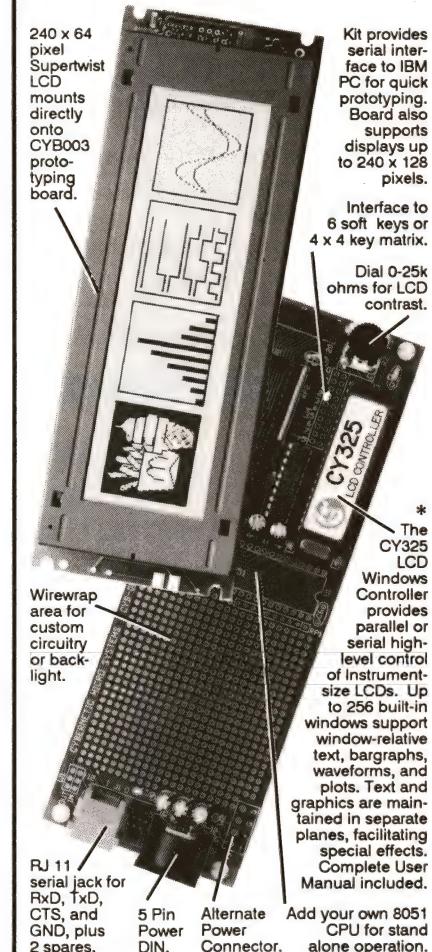
I recently read "Distributed power takes center stage" (EDN Asia, August 1994); it is a good article that covers a lot of technical issues on distributed power. (*Ed note: This article appeared in EDN Asia and EDN concurrently; see "Distributed power: Where the power meets the load," April 28, 1994, pg 54.*)

However, I have found that the section "Constant vs variable frequency," which compares the relative merits of quasiresonant- and PWM-conversion techniques, has several points that were unfavorable toward PWM techniques: 1. "According to Vicor, the efficiency of PWM converters is usually lower than that of similar-capacity resonant converters."

Efficiency of a power converter is a complicated performance indicator that depends on many circuit and operation parameters. To simplify the discussion, a PWM converter has lower

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conduction losses but higher switching losses than a quasiresonant converter (QRC) at the same switching frequency. Since switching losses are proportional to switching frequency, the power losses in a PWM converter exceed QRC above a certain switching frequency (approximately 500 kHz in practice). On the other hand, the high conduction losses in QRCs make them less efficient than their PWM counterparts at lower switching frequencies. Thus, obtain the best efficiency by using a

"low" switching frequency for a PWM converter and a "high" switching frequency for a QRC. The important job for the power-supply design engineer is to optimize a design at the chosen switching frequency. When the switching frequency is optimized, the PWM converter and QRC have similar efficiencies, which can be observed from the efficiency figure in the converter's data sheet. Therefore, the statement should read: "The efficiency of PWM and quasiresonant converters is similar

if their designs are optimized."

2. "Vicor also notes that a PWM converter's efficiency drops rapidly with load."

Since the power dissipation in the power MOSFETs and rectifiers (and even the wires) of a power converter increase with increased current passing through, the power converter's power losses inevitably increase with increased output current—regardless of whether or not the converter is using PWM or QRC techniques. Again, such characteristics can be observed from the inverted-V shape of the efficiency-load curve of most power converters. Thus, the statement should read: "Most converters' efficiency drops with increased load."

3. "PWM converters'...output ripple increases with load."

A flyback-type converter has output-ripple increase with load current, no matter if it is PWM flyback or quasiresonant flyback. On the other hand, output ripple of forward or bridge-type converters is constant, independent of load current, no matter if it is a PWM forward/bridge or quasiresonant forward/bridge. Therefore, the statement should read: "Whether output ripple of power converters increases with load depends on converter topology rather than conversion technique."

PWM- and quasiresonant-conversion technologies have been around for 20 and 10 years, respectively. Neither technology outperforms the other in all aspects, which is why both technologies are still used in [designing] products. For the power-supply user (rather than designer), the best proof for the above claims is the converter's data-sheet specifications—or a simple measurement.

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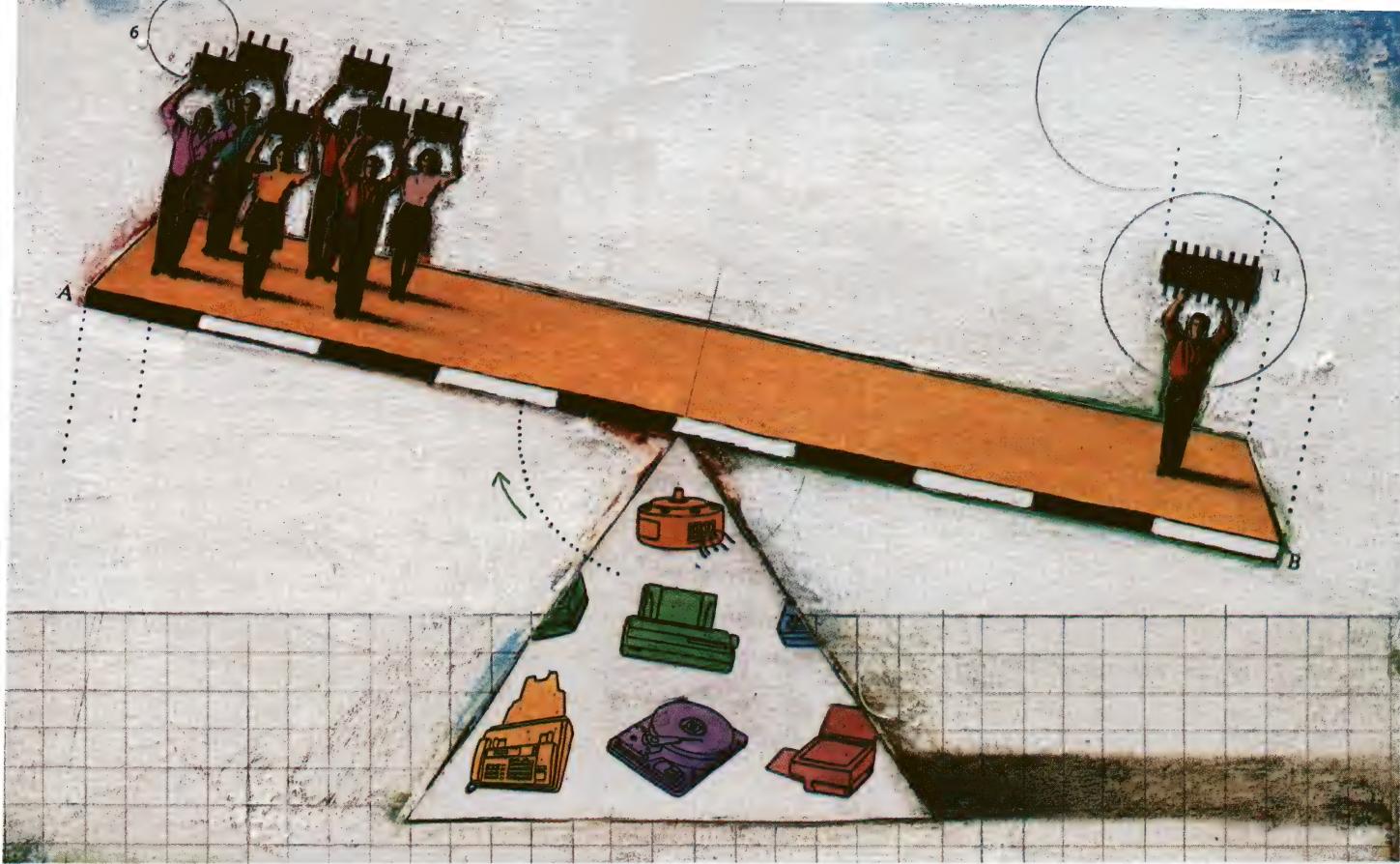
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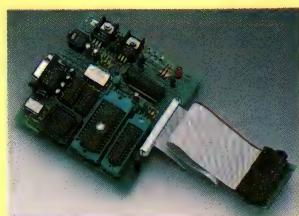


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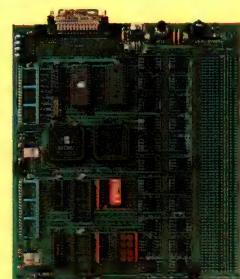
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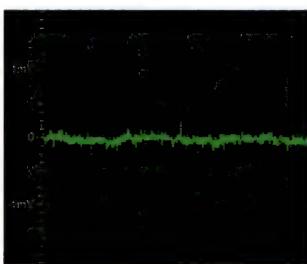
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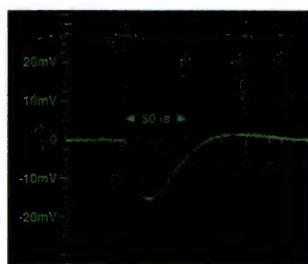
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When Congress enacts environmental laws, it should empower rule-making bodies to create standards based on input from industry experts.

Environmental regulations often place roadblocks in the way of new technologies that can significantly improve the environment. The main reason is lawmakers' and regulators' insistence on drafting regulations that require (or prohibit) the use of particular technologies. The situation with Rayovac's reusable alkaline cells (see pg 62) is a case in point. Several types of rechargeable batteries should be recycled because they contain materials such as lead and cadmium that must not be allowed to leach into the aquifers that supply drinking water. So several states set up rules that required recycling of rechargeable batteries.

Then along came Rayovac. After years of trying, it had developed a rechargeable *alkaline* battery. Lo and behold, Rayovac's reusable battery was free of the materials that pollute water supplies. Could Rayovac start selling its new batteries? Not without some hassles. You see, the regulations decreed that because the batteries were rechargeable,

they had to be recycled. But recycling would have been uneconomical—as well as unnecessary. Carried to their logical conclusion, the regulations could have prevented the sale of batteries that are safer for the environment than other types, both rechargeable and nonrechargeable.

Situations like this occur time and again in environmental law. Another example is the mandate in California and elsewhere that a percentage of vehicles produce zero emissions. Faced with this requirement and a short time frame for implementing it, the transportation industry seized on all-electric vehicles as the answer. Electrical, electronic, and battery technology almost certainly will play increasingly important roles in automobiles, but many of us have doubts about purely electric vehicles.

If you recall how electric power is generated and stored, you realize that, except maybe when the power source is hydroelectric, "nonpolluting electric vehicle" is an oxymoron. (Even hydroelectric power is not sacrosanct; environmentalists are likely to torpedo a major hydroelectric project in

Quebec, partly because it would destroy forests. Instead of mandating "zero-emission vehicles" by a certain date, why not set realistic goals for the pollutants cars generate? And include the pollution from generating propulsion energy outside of the vehicles.

Regulators seem unable to focus on the results they are trying to achieve. Few design engineers would tolerate a marketing manager's telling them which ICs to use in a new design. Selecting ICs is the designer's job. Similarly, the design community should draw the line when regulators try to dictate what technologies to use.

Things can also go sadly awry when lawmakers set performance goals. The automotive corporate-average fuel-economy (CAFE) standard is a case in point. CAFE doesn't specify technology; it specifies performance—how many miles per gallon a car manufacturer's fleet must deliver. CAFE has worked well. By encouraging rather than *requiring* the development of fuel injection and µP-based electronic ignitions, it has dramatically improved fleet mileage. But CAFE has been problematic of late because Congress—perhaps in the mistaken belief that it can repeal the laws of physics—has started tampering with the requirements. Proposed standards would force many Americans into driving tiny cars that, without big breakthroughs in safety technology, would become deathtraps.

Maybe when Congress enacts environmental laws, it should merely empower rule-making bodies to create standards based on input from industry experts. The experts won't always agree, but it's hard to imagine them doing worse than Congress. The laws and the rules that flow from them should not prescribe (or proscribe) technical approaches. Rather, laws should articulate performance *goals*—not requirements. This approach would free the engineering community to create designs that meet truly significant objectives. Monitoring conformance to results-oriented regulations could take more work than monitoring conformance to mandates that require the use—or avoidance—of particular technologies. But focusing on results would be far more effective because it would not tie designers' hands or stifle creativity.

DAN STRASSBERG, SENIOR TECHNICAL EDITOR

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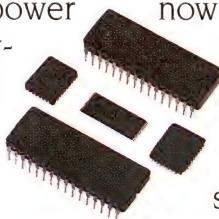
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CPUs, chip sets, and BIOS join to GREEN YOUR PC

MARKUS LEVY, TECHNICAL EDITOR



Everybody's doing it. The "green PC" no longer represents a niche market. Green PCs were first conceived and developed a few years ago by just a handful of pioneering companies. At that time, many argued that the motivation for developing green PCs was market-oriented, because customers weren't actively seeking to purchase these types of computers. Today, green PCs—and the components they comprise—proliferate every segment of the computer industry, including printers, fax machines, and a range of office equipment. The good news is that computer manufacturers are able to green their machines at little or no cost to the consumer. And the great news is the very positive impact this move has for our environment (see box, "PCs impacting the environment").

Although many designers may not currently be involved in developing green PCs, a time will come

when we'll all at least be using them. So, regardless of your level of involvement, this article offers some insight into what's happening under the hood of your power-managed computer.

Conception of the green PC

Approximately four years ago, Phoenix Technologies and Intel conceived the 24-hour-a-day PC, later known as the green PC. Greening a PC is about saving power without sacrificing system performance. No major developments occurred in this area until 1992, when the Environmental Protection Agency (EPA) announced Energy Star, a program to encourage computer-power conservation. To be certified as Energy Star-compliant, a system must enter a low-power state when the unit is inactive (a low-power state is defined as a maximum of 30W for either the computer or the monitor). Industry pundits are hoping

Green PCs, designed to better our environment through conservation, have become the norm. Although many peripheral devices have built-in mechanisms to manage power automatically, the majority of a system's green capability can be attributed to the CPU, its associated chip set, and the BIOS.

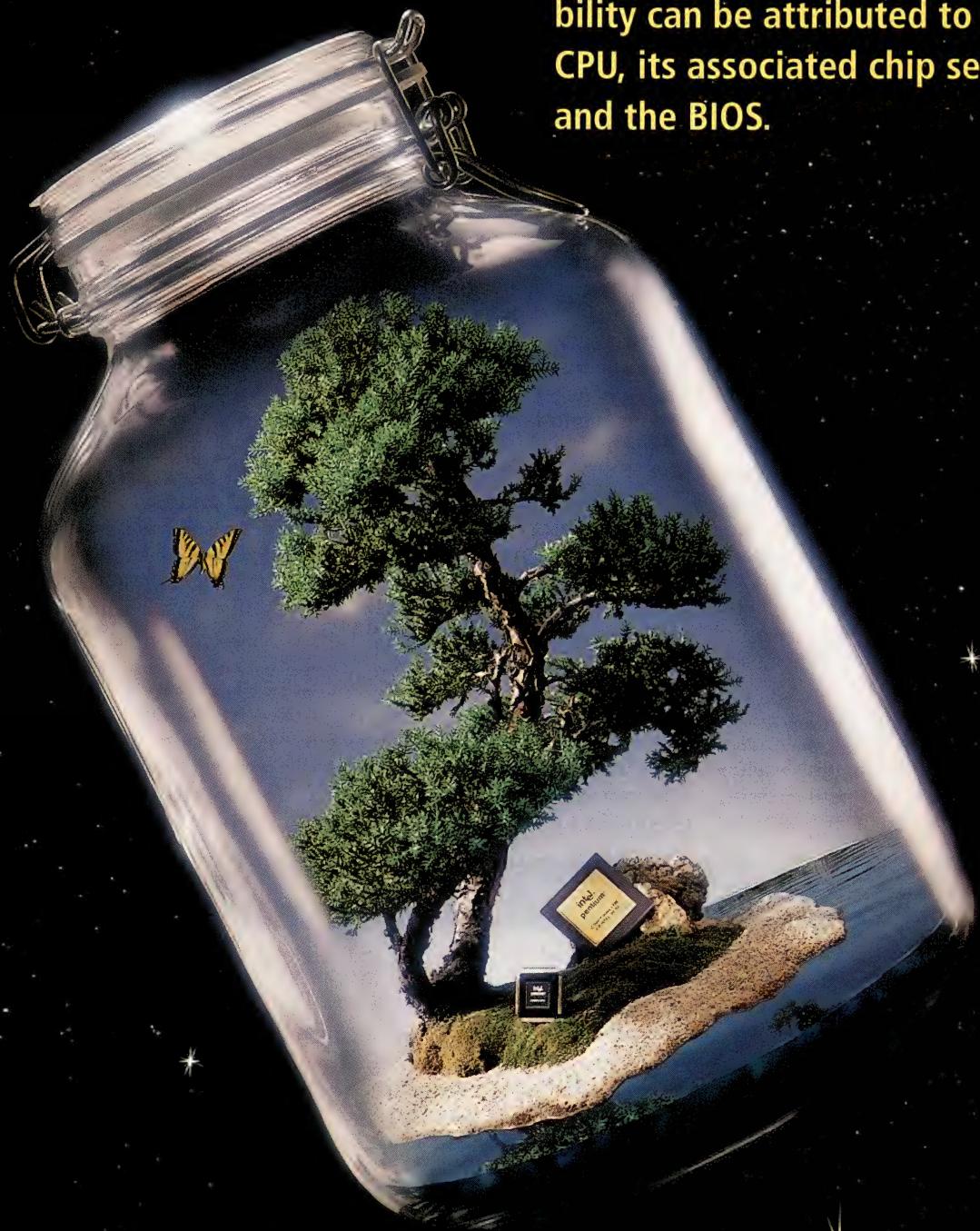


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GREEN PC

for a second phase that lowers this number, because many 486 systems meet this specification even without power-management techniques. Nonetheless, compared with the typical 160W a combined computer/monitor operating in the active mode consumes, 30W represents a big savings. And many computer and monitor manufacturers are developing equipment that consumes far less than 30W.

Energy Star is a self-policing program: an OEM must perform all of its own tests and report accurate results. In some cases where OEMs have reported incorrect information, the companies had to modify equipment or remove the Energy Star logo. To remove ambiguities in the qualification process, the EPA defined power-consumption measuring procedures. These procedures specify test conditions ranging from ambient temperature to line impedance. As the EPA forewarned, a range of watt meters is available (some of which are inadequate), so exercise care when making your selection. Some selection criteria must be based on the meter's crest factor, frequency response, resolution, accuracy, and calibration capability.

Power-consumption profiling

In a green PC, the CPU, its associated chip set, and the BIOS have a synergistic relationship in governing power management for the entire computer system. To achieve the highest level of power management and performance, a green PC design builds a complex rela-

tionship among these three components. The BIOS and chip set must monitor system activity and determine when it's appropriate to shut down the various computer subsystems. Understanding this relationship is perhaps the key—and most difficult—aspect of power management; it's more an art than a science.

A computer system comprises many devices, including the CPU, memory, keyboard, monitor, disk drive, and so on. By examining power consumption for each of these devices separately, you learn the relative impact that each device has on the system's overall power consumption. For example, you may not be surprised to see memory consuming far less power than the disk drive or CPU. Use this power profile to determine where to focus your energy when applying power-management techniques to a design. Obviously for a battery-powered computer, the goal is to squeeze every possible (and practical) power-saving source. But in a desktop computer, the primary goal should be to target the major power hogs.

The CPU is one of those power hogs, where processors such as the Pentium can consume as much as 10 to 15W in active mode. The most obvious, but not necessarily the easiest (from a manufacturing and design standpoint), means of reducing a CPU's power consumption is to reduce its operating voltage. Manufacturers built first-generation CPUs on a 5V technology; but soon most 486- and 586-class processors will be built on a 3.3V process. Originally, CPU vendors obtained 3.3V

versions by characterizing 5V devices at the lower voltage. However, in order to pass 5V parts off as 3.3V parts, they significantly derated specified operating frequencies of the 3.3V CPUs.

Newer CPUs, especially those running at 100 MHz, require 3.3V to permit faster CMOS switching times and to reduce heat generation. Today, the majority of 3.3V devices are built as 3.3V devices from the ground up, but they have 5V-tolerant outputs to support the readily available 5V logic that still dominates a PC's motherboard. Some 486 CPUs, such as the Cyrix DX2-V66 and DX2-V80, require a nominal voltage of 4V; the system needs a voltage regulator to supply this nonstandard voltage.

Current and future generations of CPUs have automatic built-in circuitry to disable clocking to nonactive execution units. For example, CPU designers commonly apply this technique to the floating-point unit, which may not always have an instruction flowing through it.

The manufacturers of 486 and Pentium processors, such as AMD, Cyrix, Intel, and Texas Instruments, have integrated several mechanisms to help achieve lower power consumption. Although these mechanisms provide similar end results, it's an interesting exercise to sort through their differences.

CPU clock control

The amount of power a CPU's circuitry consumes is linearly related to its operating frequency, $P=CV^2f$, where C is the device's capacitance, V is the difference between high and low voltage,

PCs IMPACTING THE ENVIRONMENT

Computers make up the fastest growing electricity load in the business world. The EPA has stated that a typical computer system (combined CPU, monitor, and printer) consumes 451 kWhr annually. This figure is based on a typical eight-hour workday, with 240 workdays per year. And, when compared with the 2059 kWhr per year for the system running 24 hours per day for 365 days, this represents the usage model of approximately 40% of the computers in operation. With 140 million PCs in the world today, this number expands to 153 billion kWhr used per year; to generate this energy, it takes almost 77 million tons of coal and an estimated \$11 billion—an incredible impact on both the environment and the economy.

Last year, President Clinton endorsed the EPA's Energy Star program. His directive mandates that the federal government, the largest consumer of computers in the world, will purchase only Energy Star-compliant PCs. This move will save the federal government \$40 million per year on reduced electricity costs; it also frees up tax dollars for other spending.

To learn more about the EPA Energy Star Computers Program, contact Jeff Webb, the Environmental Protection Agency, Energy Star, US EPA-6202J, 401 M St SW, Washington, DC 20460. Or, request an Energy Star information packet from the EPA Energy Star fax line at (202) 223-9659.

TABLE 1—REPRESENTATIVE GREEN CHIP SETS FOR 486S AND PENTIUM CHIPS

Device name	Number of chips	Processors (SMI support)	Bus*	Voltage at CPU interface	8-MHz clock	Clock-speed control (MHz)	Events monitored	Other power-management features
ACC Micro-2168GT	1	486 (A,C,I)	VESA	5	Yes	0 to 50	22	Susp/Resume button
-2178	1	486 (A,C,I)	VESA**	5	Yes	0 to 50	22	Susp/Resume button
-2268	1	Pentium	VESA **	5	Yes	0 to 50	22	Susp/Resume button
-2278	1	Pentium	VESA**	3.3/5 mixed	Yes	0 to 66	22	Susp/Resume button
Cypress-CY82-C599/597	2	486 (A,C,I)	PCI/VESA	5	Yes	0 to 50	11	Five user-defined timers
CY82-C691/692/693	3	Pentium	PCI	3.3/5 mixed	Yes	0 to 66	11	Five user-defined timers
Efar-EC802G and EC100	2	486 (A,C,I)	VL	5	Yes	0 to 50	30	Five watchdogs, independent timer for display, I/O trap and restart
EC810PB, EC802G, and EC100	3	486 (A,C,I)	PCI/VL	5	Yes	0 to 50	30	Five watchdogs, independent and EC100 timer for monitor, I/O trap and restart
Power Set	4	Pentium	PCI	3.3	Yes	0 to 66	20	Four watchdogs, independent timer for monitor, I/O trap and restart, user timer, power control port
IMS 5026/27/28 or Atmel 40511/512/513	4	Pentium	PCI	3.3	Yes	0 to 66	12	Eight power control pins, timers, shadow registers, clock throttling, seven modem ring resume
8848/8849 or Atmel 40411/412	2	486 (A,C,I)	PCI/VL	5	Yes	0 to 50	12	One timer
Intel-82420EX (Aries)	2	486 (I)	PCI	5	No	50	15	Clock throttling
82420ZX (Saturn)	3	486 (I)	PCI	5	No	33	15	Clock throttling
82430NX (Neptune)	4	Pentium (90/100 MHz)	PCI/EISA	3.3	No	50	15	Clock throttling
OPTi-82C802G	1	486 (A,C,I) & P24D	ISA	5	Yes	8 to 50	29	One timer, monitor and synch control
Viper	3	Pentium	PCI/VL	3.3	Yes	0 to 66	N/A	N/A
PicoPower-PT86C368 PT80C732	2	486 (A,C,I)	VL	3.3/5 hybrid	Yes	0 to 20 at 3.3V 0 to 33 at 5V	12	N/A
	4	Pentium	VL/PCI using	3.3/5 hybrid	Yes	0 to 40 at 3.3V 12	12	N/A
PT86C768	2	486 (A,C,I)	VL/PCI using	PT80C826	Yes	0 to 40 at 3.3V 0 to 50 at 5V	12	N/A
PT86C868	2	486 (A,C,I)	VL/PCI using	PT80C826	3.3/5 hybrid	0 to 40 at 3.3V 0 to 50 at 5V	12	N/A
Samsung K582C53X	3	Pentium	PCI	3.3/5	No	DC to 66	30	Four timers, expandable I/O for power control
SIS-85c496	2	486 (A,C,I)	PCI/VESA	5	Yes	0 to 50	11	Five PMU control timers, eight SMOUT, clock throttling
85C501	3	Pentium	PCI	3.3/5	No	33 to 66	11	Two watchdogs, clock throttling control
Symphony Labs-Puccini	3	Pentium	VL/PCI	3.3/5 mixed	Yes	0 to 66	7	GP I/O port, three watchdogs
Strauss	3	486 (A,C,I)	VL/PCI	5	Yes	0 to 66	7	GP I/O port controls power status of eight I/O devices, seven watchdogs
Wagner	2	486 (A,C,I)	VL	5	Yes	0 to 66	7	GP I/O port controls power status of eight I/O devices, seven watchdogs
VIA-Apollo	3	Pentium	PCI	3.3	Yes	0 to 66	12	Three activity timers, one GP timer, two idle timers, monitor synch control
Pluto	2	486 (A,C,I)	PCI	3.3	Yes	0 to 50	12	Three activity timers, one GP timer, two idle timers, monitor synch control
VLSI-VL82C483	1	486 (I)	ISA	5	Yes	8.3 to 50	24	Two watchdogs
590	3	Pentium	PCI/ISA Bridge	3.3	No	66	28	One watchdog

Notes: A=AMD, C=Cyrix, I=Intel. N/A=not available. *All support ISA. **Use ACC2188 for PCI.



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and f is the clock frequency. Within the realm of the desktop computer, slowing the clock speed was the original method used for controlling a CPU's power consumption. Nonstatic 486 processors can have clock speeds drop to 8 MHz during periods of inactivity without adversely affecting the device's operation (recently, some Intel devices have been derated to 12 MHz). Furthermore, because these devices were not static, the only way to suspend the CPU fully was to remove power. To accomplish this, the CPU's entire state had to be saved to disk. Not surprisingly, very few desktop systems implemented a full suspend. Today, most 486 and Pentium CPUs are static, allowing the clock rate to stop without state loss.

Clock-doubling and -tripling CPUs available today utilize a phase-locked loop (PLL) to synchronize the external clock signal and produce a stable clock for the CPU's internal circuitry. Jitter is an inherent problem with any PLL, typically taking 1 msec to tune itself after any input clock change of greater than 0.1%. However, usually by the time the system decides to lower the clock, the system was already idle, and the user shouldn't experience a performance degradation.

Texas Instruments' clock-doubled SX2 and SXLC2 486 CPUs incorporate a gated PLL that allows quick recovery from clock changes. A control signal within the processor allows the clock signal to bypass the PLL to enable clock frequency switching without any latency. The Enable Clock Double bit in configuration register CCRO enables PLL bypassing. In a standard implementation, these 486s run at 50 MHz internally while the system bus runs at 25 MHz. Bypassing the PLL, the CPU immediately begins running internally at 25 MHz, resulting in a two-times power reduction. While in this mode, the external clock can vary to any frequency without PLL synchronization delays.

When Intel's now-obsolete 386SL arrived on the scene in 1990, the device introduced new power-management techniques for notebook computers. Some of these techniques have evolved and proliferated throughout most 486 and Pentium products; in

addition, designers use them extensively to green most desktop computers. One of those techniques, which Intel 486s and Pentium chips use, utilizes a special pin on the CPU, called STPCLK. When the CPU samples an active STPCLK input, it stops the clock to the core but keeps the PLL active. While STPCLK is active, clock signals to memory and cache control, and external bus control units remain active, but the CPU consumes only 15% of its normal operating power. While STPCLK asserts, the Pentium still responds to interprocessor and external snoop requests. After the STPCLK signal deasserts, it takes a few clocks to return to normal execution;

attention-needing signals such as INTR, NMI, and SMI (system-management interrupt).

Another power-management mechanism the 386SL brought to the party is system-management mode (SMM), which enables code to control CPU power without having to rewrite or revamp existing operating-system software. SMM is entered via the hardware interrupt; SMI enters SMM. The SMI interrupt code can set SMM operating modes to reduce CPU and subsystem power dissipation. The SMM code, as well as the processor state, is kept in a separate memory space called system-management RAM (SM-RAM). Separating memory spaces allows the SMM to

TABLE 2—REPRESENTATIVE POWER CONSUMPTION FOR SMM-SUPPORTING CPUs¹

Device	Voltage	Frequency (MHz)	Power (W) active max	Power (W) ² suspend max	Power (W) ³ stop clock
AMD-DXL2	5	80	7.5	1.17	N/A
AMD-DX4	3.45	100	5.0	0.14	N/A
Cyrix-DX	5	66	6.6	0.17	0.005
Cyrix-DX2-V	3.45	50	2.9	0.09	0.034
Cyrix-DX2-V	3.8	66	4.4	0.13	0.038
Cyrix-DX2-V	4.0	80	5.2	0.15	0.04
Intel-Pentium	3.3	100	10.1	1.55	0.09
Intel-SX	3.3	33	1.2	0.16	0.003
Intel-SX	5	33	3.2	0.4	0.01
Intel-DX	3.3	33	1.2	0.16	0.003
Intel-DX	5	50	4.5	0.5	0.01
Intel-DX2	3.3	50	1.7	0.16	0.003
Intel-DX2	5	66	5.7	0.45	0.10
Intel-DX4	3.3	100	4.3	0.33	0.003

Notes: 1. Power numbers derived from corresponding maximum values by multiplying ICC by the device's input voltage.

2. For AMD, this number represents its 8-MHz clock-reduced mode.

3. AMD does not support this mode.

4. N/A=not applicable.

for example, the Pentium takes approximately 10 clock periods.

Cyrix and TI 486s use a slightly different method for activating such a low power mode. These processors do not have a STPCLK input. Instead they use suspend (SUSP) and suspend-acknowledge (SUSPA) signals, which power-down all logic except that associated with monitoring the CPU's RESET, HOLD, and FLUSH inputs. In addition, a HALT instruction causes all 486s and Pentium CPUs (except AMD's 5V 486s) to enter the suspend state. This suspend state will terminate on occurrence of

operate without intruding on normal CPU operation or system memory.

Using SMM in desktops has led to the distinction between light- and dark-green PCs. Light green refers to systems that rely strictly on the keyboard or mouse to wake them. This relationship presents a limitation for unattended systems on networks or with modems on autoanswer that need to be awakened by other I/O activity. Using SMM, dark-green PCs can wake up on any I/O activity that generates an SMI.

The method of SMM implementation varies among different 486 man-



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ufacturers. Regardless of the implementation, SMI execution involves four distinct phases:

1. An SMI signal is generated in response to system interrupts that monitor system activity or inactivity. The SMI is the highest priority non-maskable interrupt (higher than NMI). This interrupt cannot be reentered, and the CPU won't recognize additional SMIs until exiting from SMM.

2. The processor automatically saves its state to a fixed location within the SM-RAM space; this location varies for each manufacturer's processor. For example, AMD 486s save the processor state in the address range of 60000H-601A7H. TI's CPUs save at the top of the defined SMM space. This state-saving process is similar to a normal interrupt except that an SMI goes well beyond saving the current execution point and

status. The amount of saved information, and therefore the time to enter SMM, varies per manufacturer.

3. The SMM code executes out of SM-RAM (Fig 1). This code, which is contained in the SM-RAM, must be initialized prior to first execution of an SMI.

4. An SMI terminates by executing a new instruction called Resume Normal Mode (RSM). This operation restores the original processor state, and normal operation resumes. Of course, if the HALT instruction were executed in the SMM handler, the CPU would be stuck in the SMI until a non-SMI occurs.

The SMM implementation, first appearing on Intel's SL products, has now proliferated throughout the company's entire 486 and Pentium product lines. For this reason, Intel refers to current 486s as SL-enhanced versions; their implementation utilizes two pins,

SMI and SMI active (SMIACT). After the CPU recognizes the SMI, it asserts SMIACT, which the system logic uses to decode accesses to the separate SM-RAM. All other bus signals are identical to normal access mode. Texas Instruments' 486s use a similar approach with SMI and SMADS (address strobe) signals. While in SMM, TI 486s can use new instructions they've added to access non-SM-RAM; during these accesses, the CPUs generate the standard ADS signal while SMADS remains inactive.

AMD was first to implement SMM in a non-SL device, but, unlike Intel's approach, AMD chose a three-pin implementation. After the CPU recognizes the SMI, it begins driving the SMI signal to indicate to the system that it has entered into SMM. However, this signal should not be used to qualify SMM accesses because it remains active

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even when using the special instructions that access non-SM-RAM. The CPU uses two additional pins, SMI address status (SMI-ADS) and SMI ready (SMIRDY), for bus cycles to the SM-RAM. These two pins are analogous to ADS and RDY used in normal bus cycles.

One final note on CPU power management: next-generation, 586-class processors from AMD and Cyrix are expected to be pin compatible with Intel's Pentium (including SMI, SMI-ACT, and STPCLK). The implementation may differ internally, but, at least from a socket perspective, this compatibility allows easier acceptance into the already established Pentium market.

Green chip sets

Chip sets with power-management capability originally targeted notebook computers. Some of these notebook-chip-set manufacturers still sell these enhanced power-managed devices for green-PC designs, and others have either upgraded their existing desktop chip sets or developed entirely new green devices. The most noticeable differences between notebook and green-PC chip sets are the number of peripheral devices the chip sets monitor or control or the number of power-managed modes (ie, sleep, doze, etc). In a notebook computer, where every drop of battery life is crucial and customers are willing to pay a premium, the chip sets tend to be more robust. However, as the competition heats up, chip-set manufacturers are adding more capabilities (at lower prices) to help differentiate their products. You'll find this especially true in the mature 486 market.

The chip sets are actually the workhorses that control a system's power management. At the simplest level, they provide SMI, STPCLK, and SUSP signals. They also offer hardware monitoring and control of various system activities. Almost all chip-set manufacturers have devices that support green-PC designs. Focusing

on power-management capabilities, each green chip set has variations of the following:

- SMM support: As a minimum, all chip sets that perform this function support Intel's SMI/SMI-ACT approach. Most chip sets also support the three-pin AMD and Cyrix approach by multiplexing functionality on certain pins. There are special registers within the chip sets for selecting mechanisms, and the system BIOS is responsible for programming the registers on system initialization. BIOSs that support this capability contain algorithms to determine what type of CPU is present. This function allows PC OEMs one-stop shopping when purchasing a BIOS that works with any processor.

- Most chip sets support an "auto-green" mode to accommodate non-SL-enhanced and nonstatic CPUs. Because these CPUs are not static devices and because they have no SMM capability, this mode slows the CPU's clock to 8 MHz. Other related features may include CPU clock-scaling, throttling, and stop-clock control. Most green chip sets support the various software-controlled power-level modes such as doze, sleep, suspend, full speed, etc (Fig 2).

- All chip sets have one or more timers used in conjunction with hardware inputs to monitor system events.

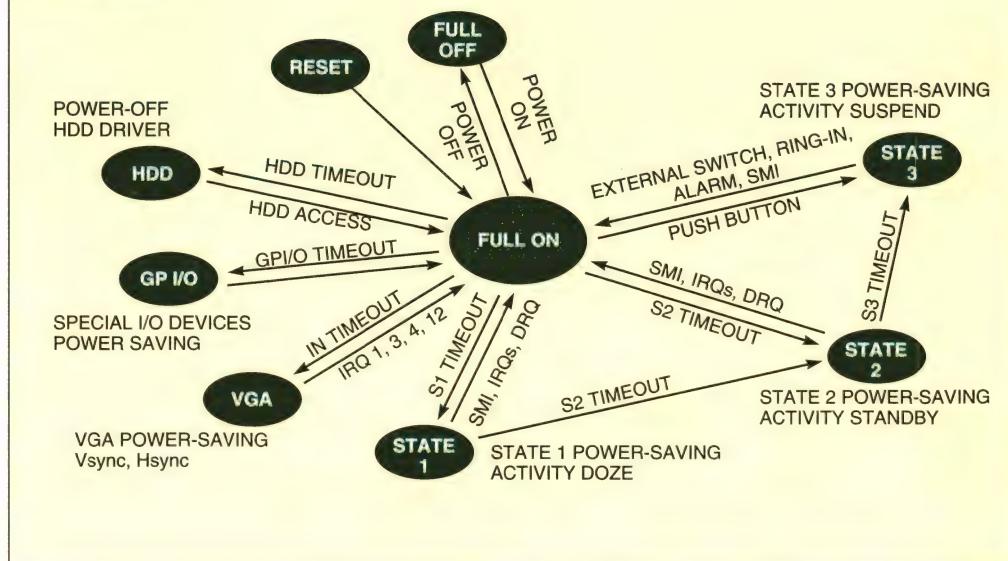
These events represent system accesses to video, floppy and HDD, serial and parallel ports, keyboard, DMA, an external input, and general-purpose memory and I/O. For an example of how this works, consider memory-access monitoring. At system initialization, the BIOS programs a specific register (or registers) within the chip set with a certain memory address range. It will also program a corresponding timer with a time-out value; this value may be user-determined or supplied as a system default and typically ranges from 1 sec to 300 minutes. The chip set monitors every access to this memory range, and each time it's accessed, the timer resets. If the memory is not accessed within the period of the time-out value, the chip set generates an SMI, causing the CPU to enter SMM and perhaps shut off power to memory.

- For those of you who leave your PC running while you go out for lunch, some chip sets include an asynchronous input, referred to as external SMI, which connects to a "coffee-break" button on the PC.

Software's role

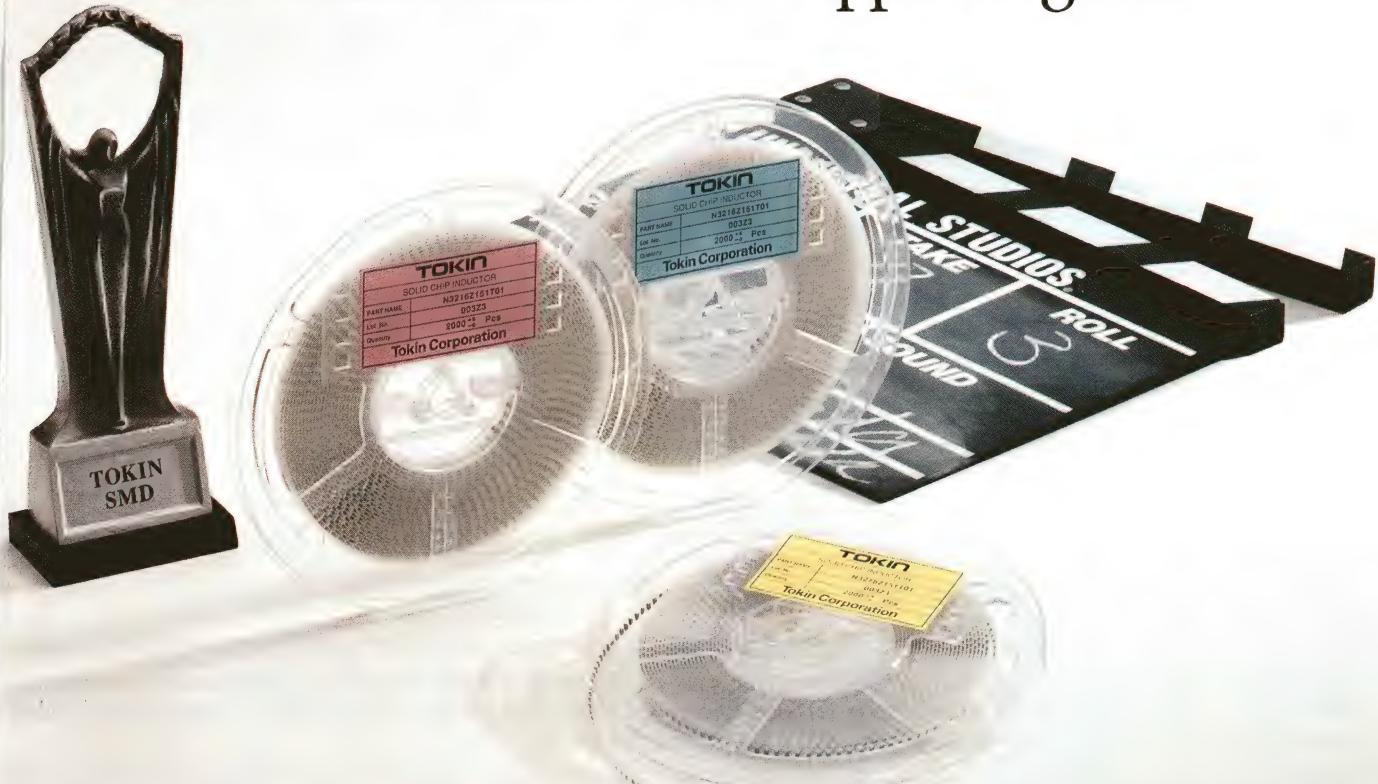
The system BIOS directly supports the hardware features of a chip set as well as the different CPUs. Although some PC OEMs have their own BIOS

FIGURE 1



Implementations of an SMI handler vary depending on the chip set, CPU, system peripherals, BIOS, or any OEM differentiating features.

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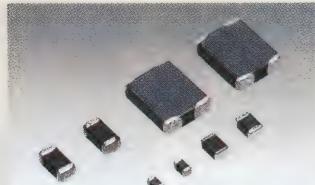
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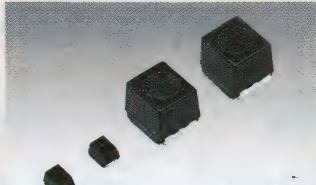
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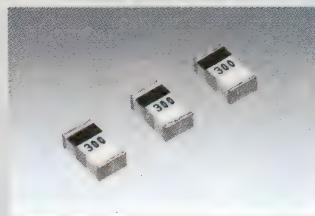
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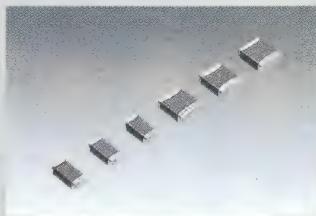
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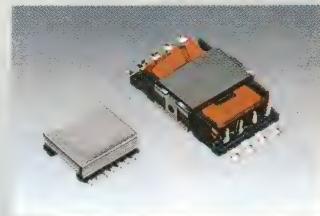
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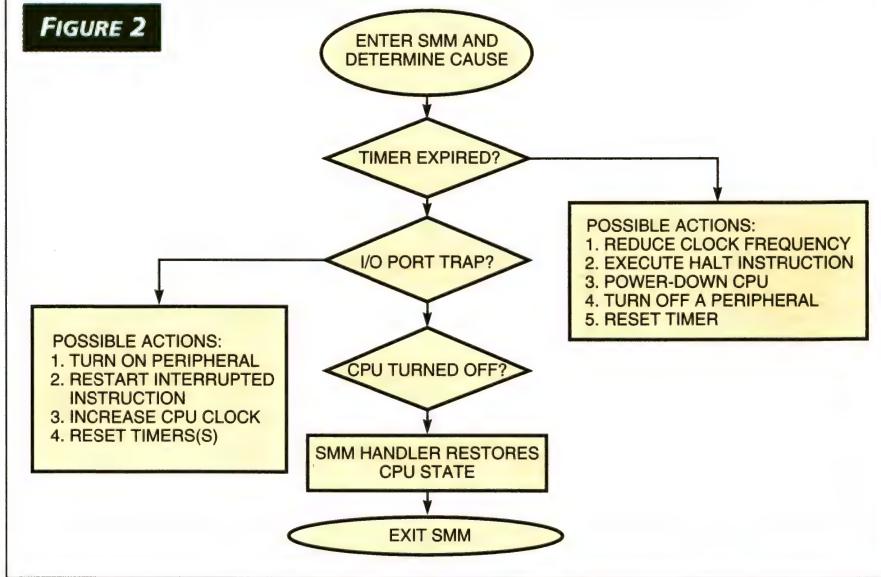


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groups, most OEMs use the services of the four major BIOS vendors (American Megatrends Inc, Award Software, Phoenix Technologies, and SystemSoft Corp), whose products support most commercially available chip sets and their power-management features.

Microsoft, Intel, and Phoenix defined an application-program interface called Advanced Power Management (APM), which lets an application running Windows 3.1 communicate with the power-management portion of a system's BIOS. During system software operation, the operating system or application program, which uses the APM to pass control to the BIOS, can detect an idle condition. The BIOS, in turn, writes a special command to the chip set. The chip set then generates an SMI to the CPU, causing it to enter SMM, which begins by determining the

FIGURE 2



ALI's M1429G is a green chip set for the 486. The chip set accommodates many common software-controlled power-level modes. These modes include the usual doze, suspend, standby, and full speed.

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cause of the SMI. In this case, the cause is determined as a request for global or local standby. Local standby refers to device-specific activities (or lack of) such as the hard drive. Global standby is platform-wide and often results in turning off the CPU.

On a desktop PC, the open architecture makes it difficult to enter into a completely suspended state. The danger stems from certain add-in cards or PCMCIA cards. Ethernet cards are one such example, because the suspend state severs the network connection. To handle this, the BIOS vendors are working with the OS providers to make "green-aware" OSs that can handle turning off peripherals. This scenario is a Catch-22 because, without power, the peripheral couldn't generate an SMI, which would turn the peripheral back on. Stop-clock modulation, available with many chip sets, provides one method for eliminating this suspend

problem. The chip set can apply a duty cycle to the stop-clock signal when the system is idle (determined by the BIOS and APM); the system wakes up on a periodic basis to respond to the timer tick or to poll a network card.

An alternative benefit to being able to achieve a suspended state in the desktop is handling the problem of losing power (and having to say farewell to the document you neglected to save). Designers could build a system to use any remaining energy to save the state before going down. Although this sounds attractive, it's uncertain whether customers will opt for the added cost.

It's amazing to think about how the power-hungry, immense computer systems of our yesteryear have evolved. Today's powerful computers, small enough to fit on our desktops, with little or no effort, consume fractions of the energy. Compared with just a year

ago, you now have many hardware and software options to support your green-PC design efforts and continue the evolution.

EDN

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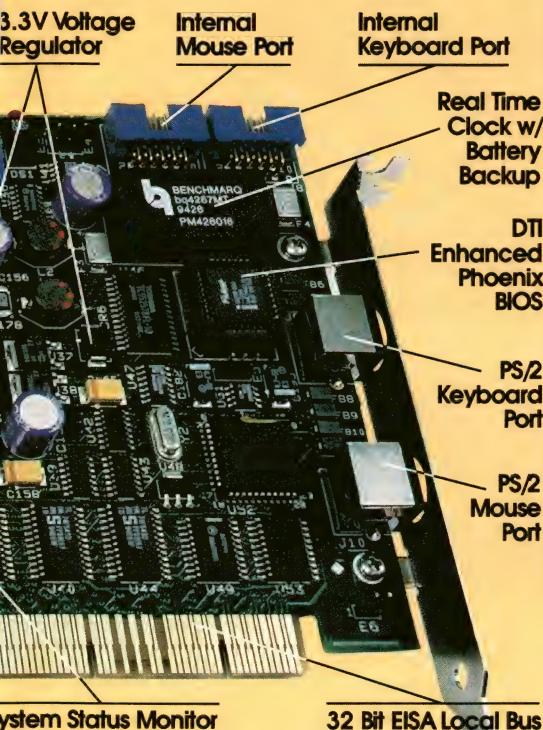
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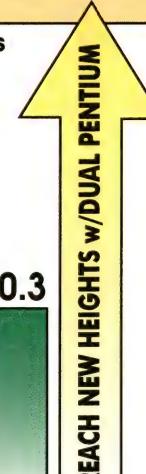
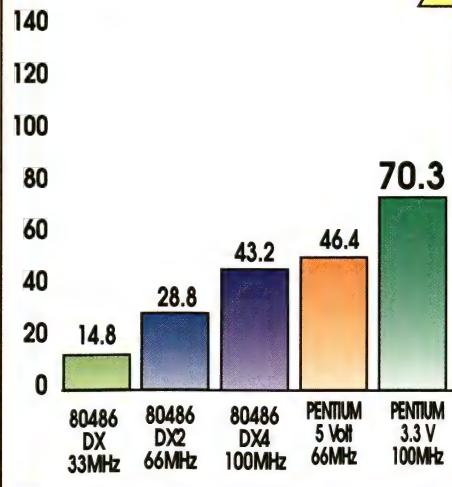
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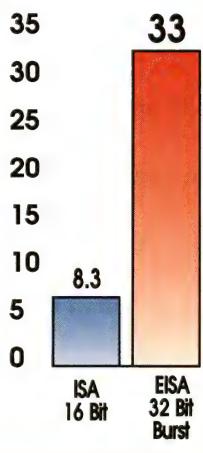
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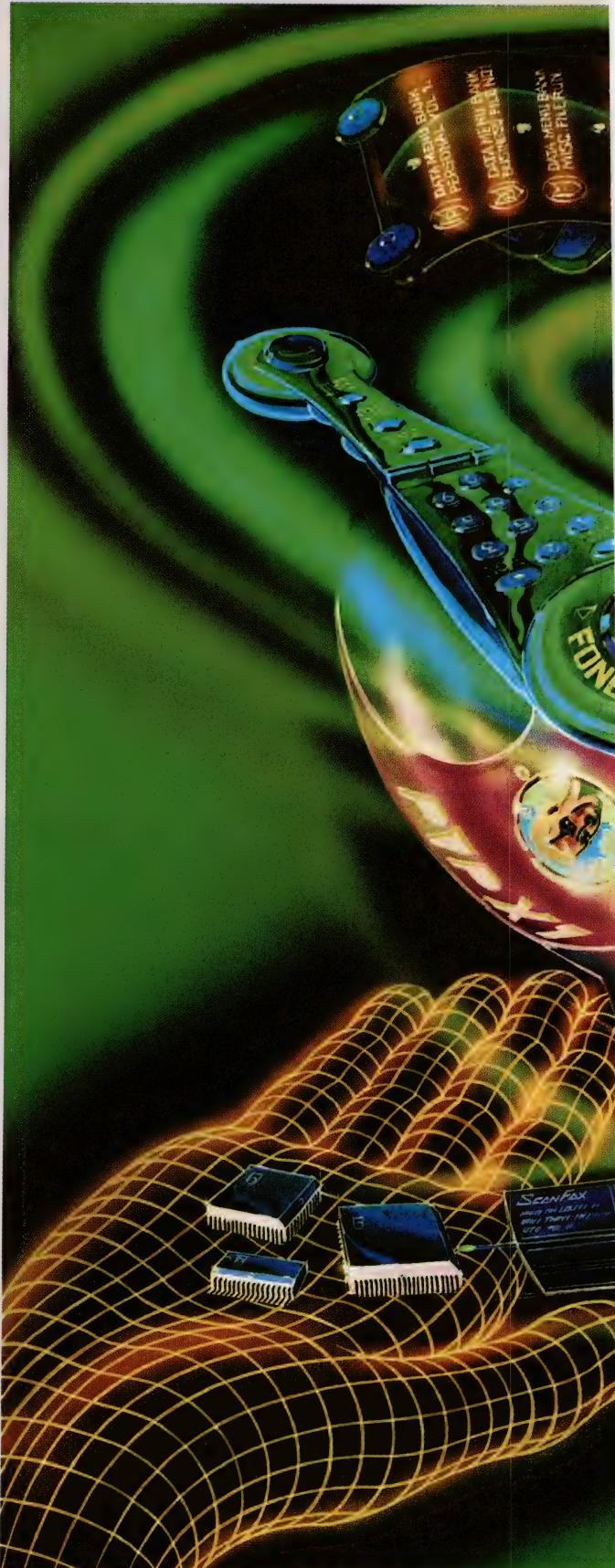
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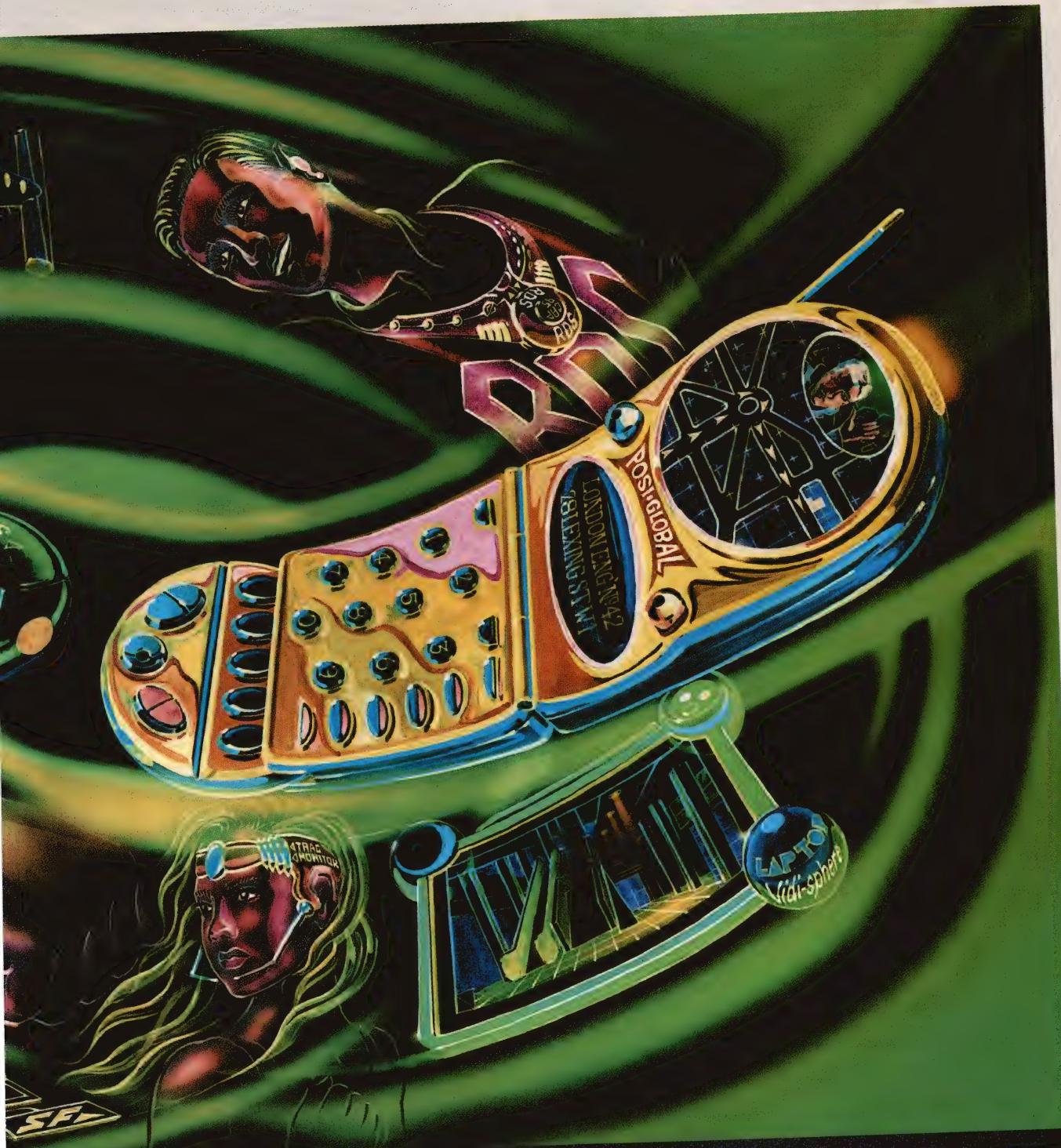
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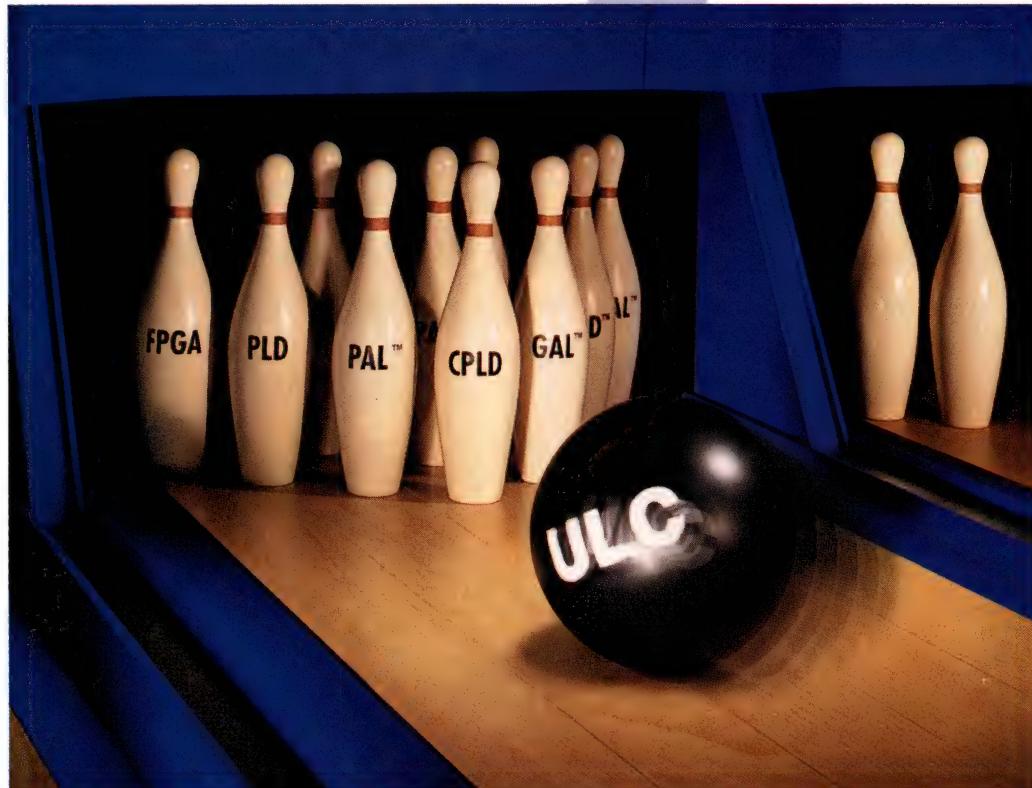


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Environmental concerns are changing much in our society—including the design of portable electronic products.

GREEN BATTERIES: *changing the rules for design*

DAN STRASSBERG, SENIOR TECHNICAL EDITOR



Designing battery-powered electronic products—especially battery-powered consumer electronic products—will never be the same as it used to be. A decade or so ago, few people thought about the toxic materials within many batteries or what happens when those materials enter the waste stream. Efforts to manage such materials now affect how manufacturers are (or should be) designing battery-powered products. Reducing the use of toxic materials has caused changes in certain types of batteries and the disappearance of others. (See box, "Where have all the Hg cells gone?") Most of all, because recycling seems to be the best way to deal with several kinds of nonautomotive rechargeable batteries, the battery industry has had to make lasting changes in some of its methods.

Generally, manufacturers should no longer design products in ways that keep users from easily replacing "worn-out" rechargeable batteries. This is the case with consumer products. For these, several states have enacted laws or adopted regulations that require easy battery replacement. Having such rules in even one populous state was enough to discourage manufacturers from designing products that users would have to discard when the batteries no longer could hold a charge. (For example, some manufacturers used to make cordless vacuums this way.) The rules for industrial products are less clear-cut, but there appear to be few good reasons to design such products with rechargeable batteries that users can't replace.

In addition, manufacturers must comply with labeling requirements: The chemistry of rechargeable batteries (NiCd, for



The easiest way to tell if the Rechargeable Battery Recycling Corp's (RBRC's) industrywide recycling program handles a rechargeable battery is to look for the RBRC's seal on the battery, the unit that uses it, and the unit's packaging. The battery's chemistry (NiCd, in this case) appears beneath the seal. Variations of the seal allow its use in several sizes, although the seal doesn't fit on some very small cells. Manufacturers of products that use such tiny cells must place the seal near the battery.

GREEN BATTERIES

example) must appear on the outside of a product containing the battery, on the product's packaging, and on the batteries themselves. If a battery is too small to bear the chemistry markings, the equipment manufacturer must mark the chemistry on the part to which users attach replacement batteries.

Bye-bye, soldered-in batteries

Soldering a battery to a pc board is no longer a good idea. It certainly isn't a good idea in a consumer product that uses a battery requiring recycling or reclamation. Sure, you can claim that a whole plug-in board is recyclable, but you could have problems getting battery recyclers to accept an assembly of which a battery is but a small part. If recyclers won't handle the assembly or if they balk at doing so at an affordable price, your company will probably have to set up its own recycling program. An interesting question is how recyclers will deal with "smart-batteries" (Ref 1), which include μ Ps and LCDs.

SGS-Thomson's Snaphat package (Fig 1) appears perfect for making pc-board-mounted batteries replaceable. The company developed Snaphat for reasons unrelated to recycling. The



Although developed for purposes unrelated to recycling and currently available only with nonrechargeable batteries, SGS-Thomson's Snaphat package could be used for rechargeable batteries that require recycling. Unlike batteries soldered to pc boards, Snaphat batteries snap out, obviating the need to recycle whole boards.

package enables designers to place non-rechargeable lithium (Li) batteries on surface-mount pc boards where reflow soldering would otherwise expose the batteries to excessive temperatures. Such nonrechargeable batteries are currently the only ones available in the Snaphat package. There are two types,

each designed for a specific IC. Prices begin at \$1.76 (10,000). Use of the package for rechargeable batteries that require recycling could solve a major problem, however.

Compared with many other industries, the battery industry has acted responsibly in the current climate of

WHERE HAVE ALL THE Hg CELLS GONE?

Mercury (actually, mercuric-oxide—HgO) button cells were nice. They had this neat characteristic: Their terminal voltage stayed nearly constant at 1.34V right to the end of their life, when it would drop precipitously. With these cells, you didn't need a voltage regulator, even for such voltage-sensitive applications as powering a light meter in a camera. Another favorite application was as a power source for hearing aids. There, the constant output voltage made it unnecessary to adjust the volume as the cells aged.

Alas, such cells are just about extinct because of their Hg content. Although Varta and perhaps others continue to supply them (see box, "For free information..."), 13 states have banned the sale of these cells. So, now what? The savior of this situation is product obsolescence. Hearing aids have a relatively limited life. Technological advances render them obsolete after a few years, and the frailty that results from the aids' high level of miniaturization lead to their eventual deterioration. When a hearing aid reaches the end of its life, the user purchases a new hearing aid that uses another kind of battery.

Cameras are a different story. They can have very long lives. Moreover, users of these (sometimes nearly priceless) inanimate objects develop relationships with them that perhaps only owners of English and Italian automobiles can appreciate.

What do you do when the time comes to replace the Hg cell that runs the light meter in a no-longer-manufactured camera to which you've become attached?

The day is fast approaching when you will have only a few choices: Although using an external light meter is an option in many cases, using one changes the camera's "feel." Some cameras may be able to use silver-oxide button cells, even though such cells' output (1.85V, theoretically) is somewhat higher and their life is not equivalent. Or you can put the camera on a shelf or donate it to a museum where others can admire it. A collector might even be willing to buy it. Alternatively, if you're adept at working with miniature electronic parts, you could modify the camera to use a different type of cell and a micropower IC regulator. There is little likelihood that you would be able to fit the cell/regulator combination where the old button cell fit, however.

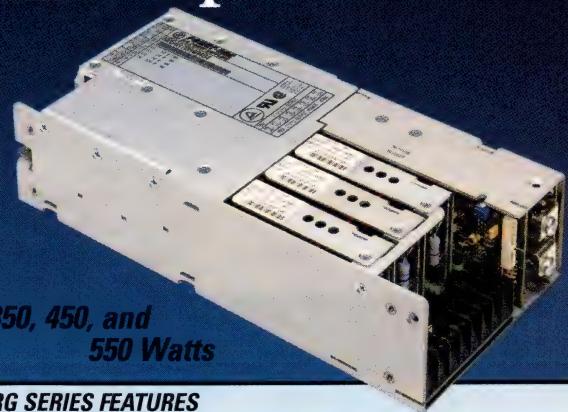
Since a lot of those old cameras still exist, you might think there'd be a business opportunity waiting to be tapped by an entrepreneur able to create a drop-in replacement for Hg button cells. Unfortunately, the market isn't large and is shrinking all the time, and the investment—particularly in production tooling—is far from trivial. As far as we can tell, until now, nobody who has looked at this "market" has been able to justify the cost of entering it.

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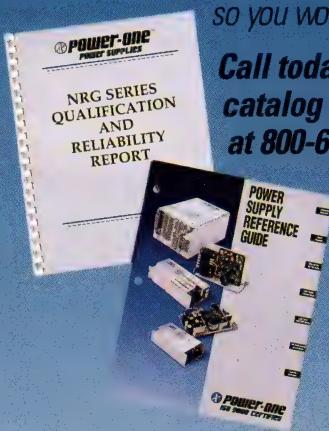
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275	5V@25A	12V@10A	12V@6A	24V@2A	NRG275-4002
275	5V@25A	12V@10A	12V@6A	48V@1A	NRG275-4003
350	5V@35A	12V@10A	12V@6A	—	NRG350-3000
350	5V@35A	12V@10A	12V@6A	5V@3A	NRG350-4000
350	5V@35A	12V@10A	12V@6A	12V@3A	NRG350-4001
350	5V@35A	12V@10A	12V@6A	24V@3A	NRG350-4002
350	5V@35A	12V@10A	12V@6A	48V@1A	NRG350-4003
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environmental concern, even though regulators have not made life particularly easy for battery vendors. Battery makers have succeeded in substantially removing mercury (Hg) from the most common nonrechargeable (primary) cells, often called dry cells: alkaline (now the most common kind) and the older "general-purpose" and "heavy-duty" types. (This article uses the terms "battery" and "cell" interchangeably. Technically, though, a cell is the fundamental building block of a battery, which comprises multiple cells.) All of these dry cells use electrodes made of manganese-dioxide (MnO_2) and zinc (Zn). The cell types differ in material purity, electrolyte composition, and construction details.

You may wonder what mercury was

doing in such batteries at all. Manufacturers added the heavy metal because it reduced hydrogen (H_2) outgassing from the electrodes. The most pronounced effect of the evolution of H_2 in these batteries was ruptured cases and leakage of corrosive electrolytes, which often ruined the product that held the battery. Manufacturers first found that they were using more Hg than they had to; initial reductions in Hg content did not affect battery characteristics. Thanks to redesigned construction and changes in the chemical additives and other materials, the only traces of Hg in dry cells today are minute amounts of impurities.

The "no-mercury-added" versions of dry cells cost users no more than their predecessors did; the new batteries also

offer greater shelf life and, in most uses, longer service life. The removal of Hg has enabled consumers, but not necessarily industrial users, to continue disposing of dry cells (and batteries that contain the cells) as ordinary household waste.

European countries, which first proposed regulating the Hg content of batteries, provided the impetus for these changes. Several US states, beginning with New Jersey and Minnesota, then promulgated their own regulations. Dry-cell manufacturers recognized that it was in their own best interest to seize the initiative; otherwise, they might have to deal with 50 sets of rules. NEMA, which includes battery manufacturers among its members, established rules on phasing Hg out of dry

REUSABLE ALKALINE: HELP THE ENVIRONMENT; ASK FOR TROUBLE

Within the past year, Rayovac began selling a battery that it and its competitors had been trying to produce for decades—a practical reusable alkaline cell. (Rayovac's brand name is Renewal.) Because these cells cannot supply high currents as well as NiCd and nickel-metal hydride (NiMH) cells, they are not a general-purpose replacement for the more familiar rechargeable units. However, manufacturers can redesign many products that use NiCd and NiMH batteries to accept reusable alkalines. And reusable alkalines work well in just about every application designed for nonrechargeable alkalines of the same size.

Reusable alkaline batteries are friendlier to the environment than the alternatives are. Unlike NiCd, probably the most familiar rechargeable in portable applications, reusable alkalines do not use cadmium or nickel. Unlike NiMH, they do not use nickel or rare-earth metals. Reusable alkalines do even less harm to the environment than do conventional alkaline batteries, with which they have much in common. Although environmentalists consider conventional alkalines safe enough not to require recycling, reusable alkalines are better yet. Because of their rechargeability, they find their way into landfills only a fraction as often.

Despite these advantages, the reusable cells didn't at first receive a warm reception from regulators. The problem was that several states' regulations called for recycling of *rechargeable* batteries, and reusable alkalines are—well—rechargeable. Because the cells are rechargeable, the regulations dictated that users had to recycle them. However, a reusable alkaline that needed to be recycled would be far less attractive than one you could just discard. Without a change in the regulations, Rayovac would not be able to sell as many, there would be fewer economies of scale, and prices would have to rise. That would further reduce the product's appeal...and its environmental benefits.

Rayovac was able to work with the regulators to get the rules changed. As a result, you can now buy Renewal cells in AAA, AA, C, and D sizes. A charger that handles four of the AAAs or AAs costs about \$15, and Rayovac claims that most users will have paid for the charger by the time they have to replace their first package of four cells. But the story just reinforces what should be painfully clear by now: All too often, environmental regulations are the worst enemy of cleaning up the environment. Moreover, regulators and lawyers whose livelihood depends upon reviewing and changing the regulations have a vested interest in maintaining this status quo. Meanwhile, the taxpayers foot the bill.



Alkaline "dry" cells are among the most environmentally friendly types, even though they must be discarded fairly often. Rayovac's Renewal reusable (rechargeable) alkaline cells are even friendlier because users don't have to discard them as often. Rayovac says that many users will have recovered the cost of the charger (about \$15 for the smaller size) by the time their first package of cells needs replacement.

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GREEN BATTERIES

cells, and the industry beat its self-imposed deadlines. Because of the success of the industry initiative, states have refrained from trying to further regulate dry cells' Hg content.

Rechargeable cells and battery packs pose a greater challenge. In electronics, the most common of these are sealed lead-acid and NiCd batteries. Many people regard the relatively new nickel-metal hydride (NiMH) batteries and even newer rechargeable Li batteries as a way around the problems of other types, especially NiCd. In fact, though, no one has yet determined whether to classify NiMH batteries as non-hazardous waste material. Nickel acts as a catalyst in incinerators; to some environmentalists, that's enough reason to classify spent NiMH batteries as hazardous.

Environmentalists are also concerned about lithium, a very active metal. There are many Li battery chemistries. Whereas environmentalists consider batteries that use some of these chemistries safe for disposal in consumer quantities, that is not generally true for industrial quantities. Even in small quantities, it is not the case for Li batteries that contain other toxic materials such as sulfur-dioxide (SO_2). BDT (see box, "For free information...") specializes in disposing of Li and other battery types.

Reclamation facilities such as International Metals Reclamation Co (also in the "For free information..." box) can recover a greater portion of the



Even the packaging of batteries is an environmental concern. Regulators—at first, in Europe—may outlaw blister packs because their combination of cardboard and plastic makes them hard to recycle. This replacement, Kodak's "all-card" package, uses no plastic but still allows consumers to see the cells through a cutout.

metal content of NiCd batteries than of NiMH ones. Thus, as with so many environmental issues, a problem's "obvious" solution (in this case, replacement of NiCd with NiMH) can turn out not to work as well as a seemingly inferior approach (recycling of NiCd cells). The automotive lead-acid-battery industry achieves recycling rates of 95% or more. If the nonautomotive-battery industry can come close to those rates with nickel-containing

rechargeable batteries, NiCd batteries will actually do less harm to the environment than the "friendlier" NiMH type.

But therein lies the challenge: establishment of a recycling infrastructure for NiCd, NiMH, and sealed lead-acid batteries used in nonautomotive products—many of them electronic. Establishment of the efficient recycling infrastructure for automotive batteries took decades.

Bureaucracies are us!

Only if you've had some experience dealing with slow-moving and sometimes-inept governmental bureaucracies are you likely to appreciate what the nonautomotive rechargeable-battery industry has gone through to establish a recycling program. Several years ago, manufacturers of NiCd and sealed lead-acid batteries recognized the need to cooperate in addressing environmental issues. That recognition eventually led to the creation of a trade association,

the Portable, Rechargeable Battery Association (PRBA).

The PRBA quickly determined that the most practical way to keep battery materials out of the waste stream was a recycling program. It was obvious that, even though recycling might eventually reduce the price of battery raw materials, recycling would initially be costly, and someone would have to pay. If each manufacturer had to establish a separate recycling program, obtaining

LOOKING AHEAD

Despite their importance to a field as dynamic and rapidly changing as portable electronics, batteries evolve rather slowly. New chemistries don't spring up overnight. Indeed, some in use today have been around for at least a century. Nevertheless, batteries continue to evolve; vendors continually make subtle improvements (removing mercury from dry cells, for example) and not-so-subtle ones (like Rayovac's development of reusable alkaline cells. See box, "Reusable alkaline: Help the environment; ask for trouble". Like Eveready's pink Energizer bunny on TV, the vendors keep on going, and going, and going in their quest to make better batteries.

Nevertheless, it would be difficult to predict that over the next year there will be great upheavals in battery technology.

Any changes that do occur are unlikely to have a major effect on the environmental friendliness of the batteries used in portable electronic equipment. The most significant development will probably be nontechnical. Expect the Rechargeable Battery Recycling Corp to move its recycling program into high gear and to work out a lot of kinks.

Over the longer term—within the first decade of the 21st century—look for technology developed for automotive batteries to filter down to portable electronics. The results will be batteries—zinc-air, perhaps—that store more energy per gram and per cubic centimeter and that do less harm to the environment than do the batteries we use today.

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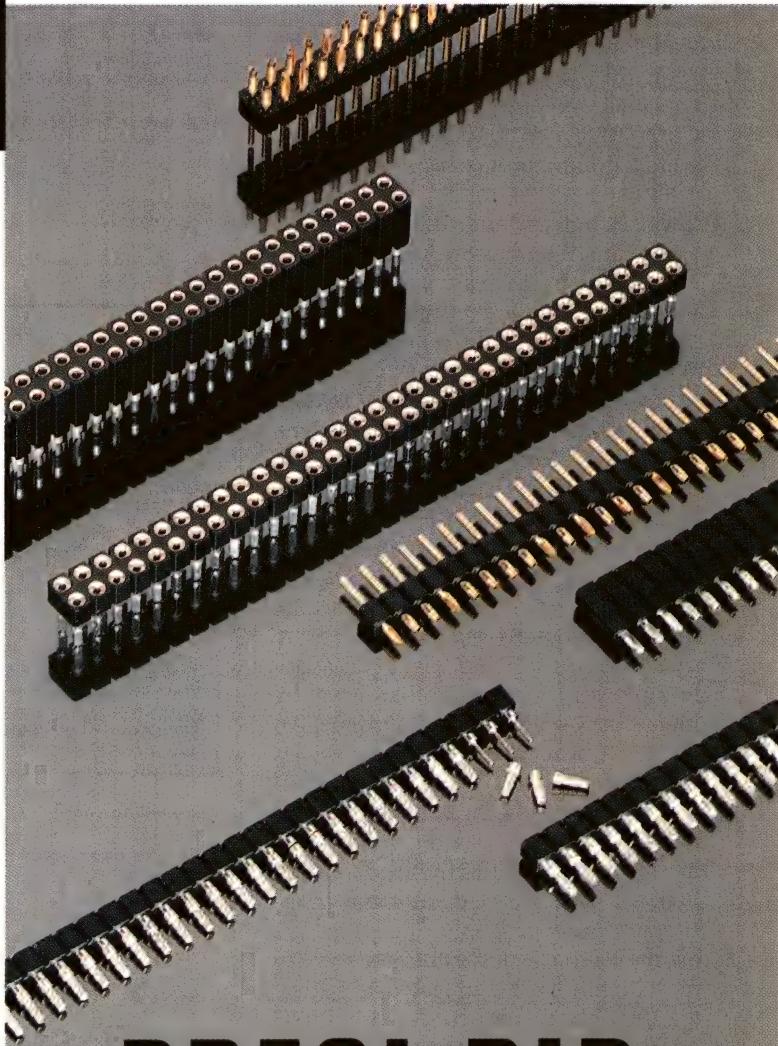
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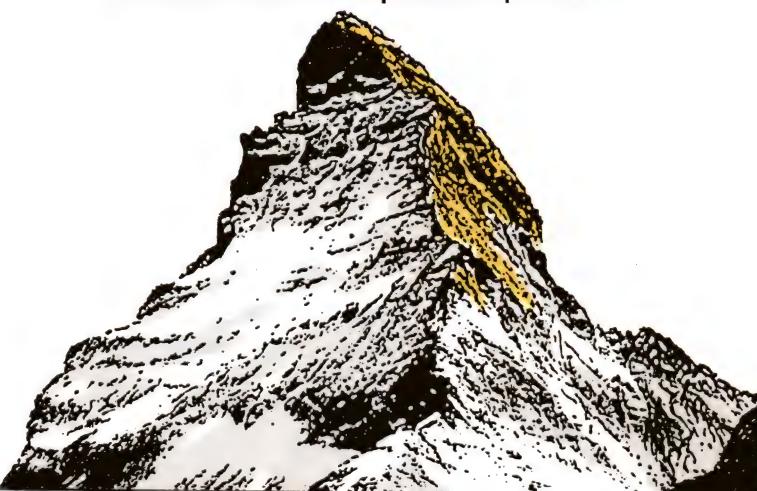
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GREEN BATTERIES

the cooperation of distributors and dealers would be more difficult—maybe impossible. In addition, there would be needless duplication, which would raise costs. Eventually, the PRBA spun off a not-for-profit corporation, the Rechargeable Battery Recycling Corp (RBRC) to manage an industry-wide recycling program.

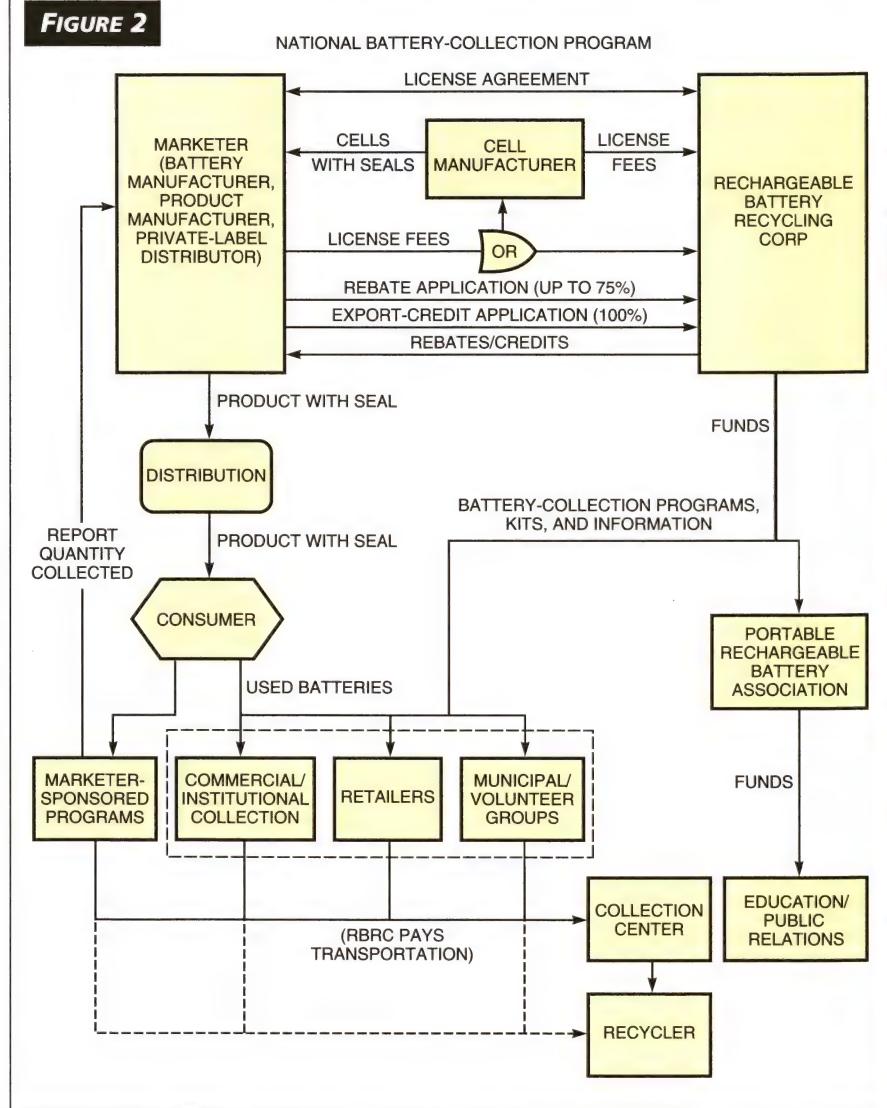
Enter the first roadblock: antitrust laws. If battery manufacturers had agreed among themselves to cover recycling costs by increasing prices, they would have been "conspiring" to raise prices, a violation of the antitrust laws. What evolved was a fairly convoluted licensing system, under which battery manufacturers, distributors, resellers, and manufacturers of equipment that uses batteries, pay royalties to the RBRC for use of its seal. The RBRC bases payments on the weight of the recyclable materials in the products a company ships. In return, the RBRC manages the recycling program (Fig 2).

Although the RBRC seal is an adaptation of the by-now-familiar recycling logo, the two differ in significance. An item that bears the "chasing arrows" is made of recycled materials, is itself recyclable, or is both. But the presence of the chasing arrows on a recyclable item isn't sufficient to indicate that the item *must* be recycled. In some cases, though, the logo implies just that. For example, many jurisdictions require recycling of NiCd and lead-acid batteries. Until the introduction of the RBRC seal, however, products that used such batteries carried no indication of this requirement—except for the chasing arrows and a written message.

On a battery, the RBRC seal shows not only that the battery is recyclable, but also that, in many places, it must not be sent to a landfill. The seal also indicates that the supplier participates in the RBRC's industrywide recycling program. So RBRC recycling centers *will* accept the battery. On a product that contains a battery, the RBRC seal signals that the landfills in many areas do not accept the battery, but RBRC recycling centers do accept it.

The next obstacles were rules of the US Environmental Protection Agency (EPA) and its state counterparts. Although intended to encourage recycling, the regulations looked as if they might have the opposite effect. For

FIGURE 2



Keeping the toxic materials in such batteries as NiCd and sealed lead acid out of the waste stream is the objective of the recycling program of the not-for-profit Rechargeable Battery Recycling Corp. Electronic products use a significant fraction of the batteries on which the RBRC focuses.

recycling to work, you must store quantities of the material you will recycle until you have enough of it to transport and process economically. But requirements for complex paperwork make bulk storage and transportation difficult and expensive. The RBRC had to work with regulators to change the rules. (The initial regulations are yet another example of how, if left unchallenged, a way of "solving" an environmental problem can actually make the problem worse.)

One of the biggest handicaps to the smooth operation of the RBRC's recycling program is that recycling and dis-

posal of batteries currently come under the purview of the states. The Resource Conservation and Reclamation Act, a federal law also called the Superfund law, does not set up hard and fast rules. The EPA regulations in this area are advisory only; state laws can preempt them.

Both the US Senate (in Bill No. S.729) and the House of Representatives (in HR.4882) have proposed legislation that would preempt state laws, thereby establishing cohesive national regulations. As this article went to press, the PRBA was encouraging interested parties throughout the industry to urge their senators and representa-

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GREEN BATTERIES

tives to enact these laws.

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ly, by the time you read this, the 1994 edition of the seminar will be history. However, the proceedings (as well as those of previous seminars) are available at \$95 per copy from Florida Educational Seminars (see below). **EDN**

You can reach Senior Technical Editor Dan Strassberg at (617) 558-4205, fax (617) 558-4470; EDN BBS EDNSTRAS Internet ednstrassberg@mcimail.com

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1. Small, Charles H, "Batteries explode into new applications and new chemistries," *EDN*, October 13, 1994, pg 63.

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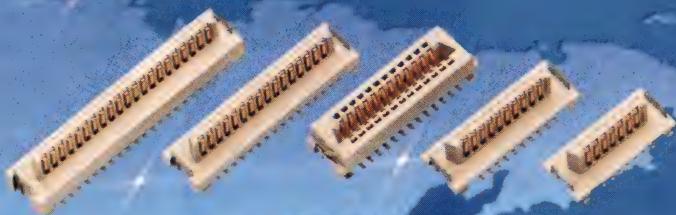
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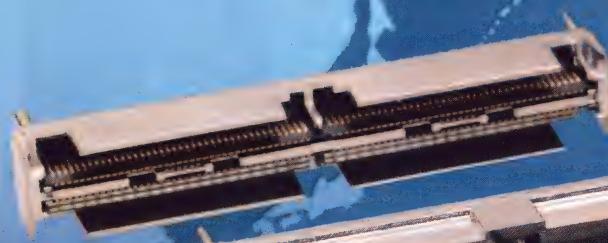
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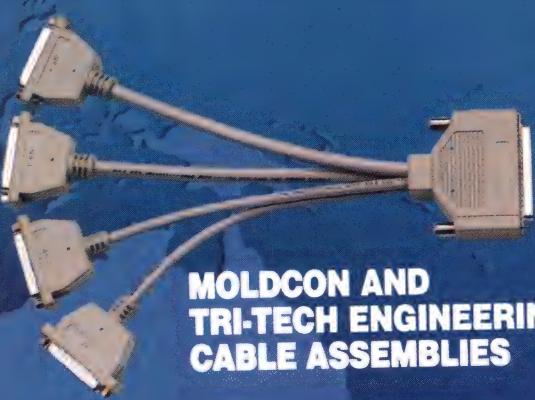
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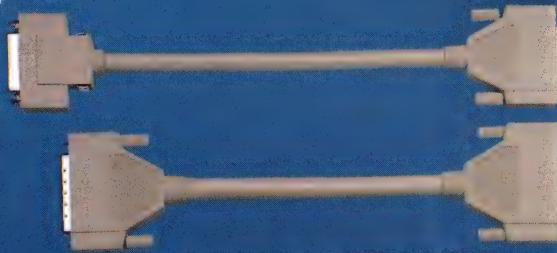
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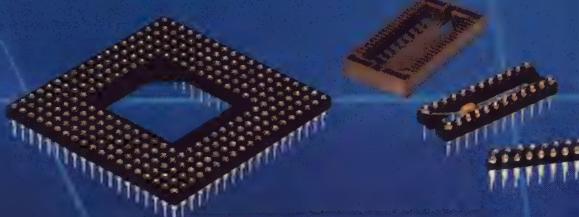
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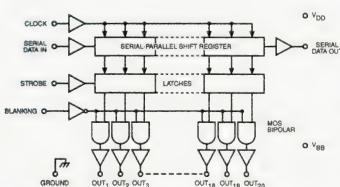
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CURRENT SHOWCASE

BiMOS II 20-Bit Serial-Input, Latched Source Drivers with Active DMOS Pull-Downs — 5812-F

The 5812-F combines a 20-bit CMOS shift register, data latches, and control circuitry with high-voltage bipolar source drivers and active DMOS pull-downs for reduced supply current requirements.

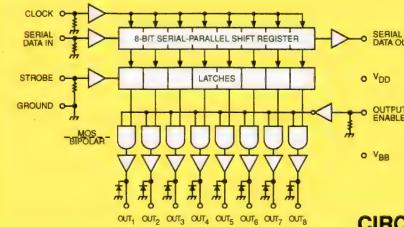
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- 60 V or 80 V Source Outputs
- Active DMOS Pull-Downs
- Low-Output Saturation Voltages
- 3.3 MHz Minimum Data Input Rate
- Reduced Supply Current Requirements



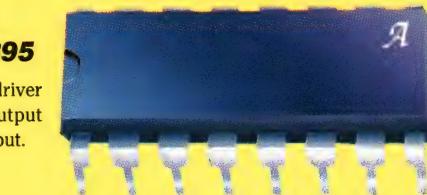
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BiMOS II 8-Bit Serial Input, Latched Source Driver — 5895

The 5895 BiMOS II serial-input, latched source driver is designed for applications emphasizing low-output saturation voltages and currents to -250 mA per output.



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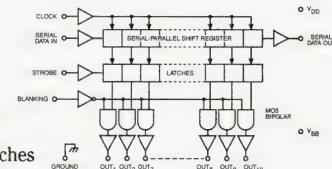


- Low Output-Saturation Voltage
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- 3.3 MHz Minimum Data-Input Rate
- Low-Power CMOS Logic & Latches

BiMOS II 10-Bit Serial-Input, Latched Source Drivers with Active DMOS Pull-Down — 5810-F

The 5810 combines 10-bit CMOS shift register and accompanying data latches, control circuitry, bipolar sourcing outputs with DMOS active pull-downs.

- High-Speed Source Drivers
- 60 V or 80 V Minimum Output Breakdown
- Active DMOS Pull-Downs
- Low Output Saturation Voltages
- Low-Power CMOS Logic and Latches
- 3.3 MHz Minimum Data Input Rate

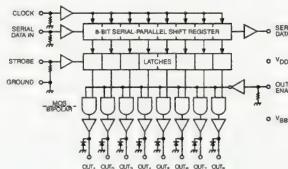


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GETTING GREEN PC BOARDS BECOMES A BURNING ISSUE

BRIAN KERRIDGE, SENIOR TECHNICAL EDITOR



If you happen to fall asleep while reading this article, and if the furniture you're resting on happens to catch fire, chances are you'll survive the incident. But nod off near a smoldering rack of pc cards, and that's

where the story will end. For, although Western legislation has long since outlawed furniture materials that burn with toxic fumes, electronic products still burn with damaging effects, and similar regulations have yet to apply.

In 1989, Siemens Corporate Research and Development, based in Erlangen, Germany, embarked on a project to study this burning problem and to develop replacement materials. The result of the company's work is a patented pc-board material, called FRN, which not only burns "greenly" but also will be in products in 1995 and looks set to replace today's widespread use of FR4 material.

Although you may not regard electronic products as generally combustible, they increasingly intermingle with flammable

objects in our offices, factories, and homes. Evidence shows that twice as many deaths occur due to a fire's toxic emissions than directly from the flames, and so the threat of injury from burning electronic products is very real. Within

electronic products, burning pc-board material causes the major environmental impact, although the effects of burning component encapsulation and IC plastic packaging are also significant. Currently, the annual worldwide volume of electronic products contains

around 350,000 tonnes of pc-board material and 100,000 tonnes of molding compounds (1 tonne=1000 kg).

These noxious emissions will take on greater environmental relevance as countries introduce stringent recycling and waste-disposal regulations. Limiting the spread of dangerous compounds during recycling and disposing of waste by incineration will become commonplace requirements. Ultimately, part of that legislation will enforce you to control the environmental impact of your designs, which means

Constituents of today's pc-board material limit flammability but exude evil gases when burning. Tomorrow's pc-board material burns cleanly and is well ahead of controlling legislation.

GREEN PC BOARDS

you'll need to consider factors affecting product destruction alongside your work on product creation (see box, "Adopting a life-cycle design mentality").

Flame-retardants kick up stink

Ironically, substances originally designed-in to pc boards and component encapsulants as flame-retardants are the very same substances at the source of the noxious emissions problem. Plastic materials are generally flame-retardant according to Underwriters Laboratories specification UL 94V-0. This specification requires that flames should extinguish less than 5 sec after you subject the material to a 10-sec burn.

Traditionally, substances designed-in to meet this specification come from the halogen group of elements, of which bromine or chlorine is a common choice. For example, regular FR4 pc-board material contains around 10% bromine compounds.

When pc-board material burns, these bromine compounds release hydrogen bromide and bromine radicals, which quench the fire by inhibiting a chain reaction with oxygen. Humans and the environment suffer because hydrogen bromide and bromine radicals are extremely corrosive and because burning generates highly toxic gases—dibenzodioxins and dibenzofuranes.

As a further twist, component-encapsulating material contains antimony trioxide as a synergist to bond bromine compounds into the chemical structure of the material. When burning, components disperse antimony-trioxide dust, which is carcinogenic.

Siemens' work in developing replacement plastics has

Table 1—Comparison of green FRN, typical FR4 pc-board material (1.6 mm), and MIL-P-13949G

Property	FRN	FR4	MIL-P-13949G
Surface resistivity (Ω) (23°C)	4×10^{11}	4×10^{12}	10^{10}
	1.5×10^{13}	7×10^{10}	10^9
Volume resistivity ($\Omega \cdot \text{cm}$) (23°C)	4.9×10^{11}	8×10^{14}	5×10^{11}
	5.4×10^{11}	8×10^{11}	10^9
Dielectric constant	4.66	4.70	5.40
Dielectric loss factor ($\tan \delta$)	0.012	0.019	0.030
Water absorption	0.33%	0.15%	0.35%
Glass transition temperature	195°C	135°C	Unspecified
Copper peel strength (35 μm)	1.7N/mm	2.0N/mm	1.4N/mm

focused on eliminating all traces of halogen and antimony trioxide while preserving structural, electrical, and processing characteristics and also retaining flame-retardancy.

For the new FRN pc-board material, Siemens uses nitrogen and phosphorous compounds to achieve flame-retardancy. These compounds have a high affinity to combine with oxygen, leaving less oxygen to sustain combustion. In fact, phosphorous compounds, in particular, further assist flame-retardancy by forming a smooth vitreous heat-insulating cocoon over the surfaces of a burning pc board. To comply with UL 94V-0, FRN material contains around 2.7% phosphorus. Burning tests at the German Research Center for Health and the Environment in Neuherberg and at the University of Bayreuth show no evidence of the release of phosphorus compounds into the atmosphere.

To add momentum to the introduction of FRN material, Siemens has enlisted the aid of other German companies, such as chemical giants Bayer and Hoechst and laminator Isola. Sample material from these companies has passed

LOOKING AHEAD

Increasingly, the principle of "producer responsibility" for the environmental impact of products will penetrate the tranquility of your design office.

To engender that principle, government authorities such as the Environmental Protection Agency in the United States and the Industry Council for Electronic Equipment Recycling in the United Kingdom are preparing the way for controlling legislation. The form of the legislation is as yet unclear, but in the European Community, proposals to impose a "disposal levy" on producers is one possibility. Nasty products will attract high levies; friendly products may escape totally.

Germany is Europe's greening force, and the principle of producer responsi-

bility is already evident there. Buyers increasingly demand that vendors take back old products when they buy anew. Germany also expects to be first with legislation (within three years), and the German auto industry already places environmental requirements on its suppliers.

In anticipation of these moves, companies are busy developing internal environmental-design policies. Siemens, for example, has implemented wide-ranging internal guidelines. As part of the program, Siemens classified the range of plastics used throughout its products into five categories ranging from "highly recommended" to "do not use." The program requires designers to seek formal levels of approval to use parts con-

taining plastics in the various categories and will phase out some categories altogether.

Eliminating halogen flame-retardants in pc-boards and discrete component encapsulants was a necessary part of the program, and you can expect Siemens to report similar progress on IC plastic packaging by the end of 1995.

To assist you in operating your own policies, companies will increasingly state the environmental impact of products, maybe through a system of labeling. Companies such as National Semiconductor, Philips Semiconductors (Ref 2), and Siemens already routinely publish data specifying the chemical content of their products.

New Product Update



REG5601
SCSI-2

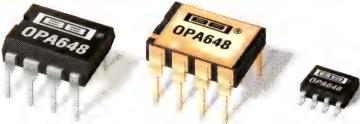
18-Line Active Terminator

CSI Termination Chip with Power-Down Mode

G5601 is an 18-line active terminator for SCSI-2 circuitry. On-chip resistors and 2.9V regulator provide the prescribed 110Ω termination for low power dissipation and high speed data transmission. An alternate source for the popular "5601" SCSI terminator. All line connections can be disconnected from the bus with a single logic control line to reduce standby power consumption. Key specs include: 2.9V current-limited and thermally protected regulator, power-down mode of $150\mu\text{A}$ max, and an output capacitance in disconnect mode of 10pF typ. REG5601 is packaged in a 28-lead surface mount package.

CIRCLE NO. 26

New



Electrometer-Grade Op Amp 1 8-pin DIP and SO-8

PA129 is an electrometer-grade op amp offered in cost-saving 8-pin DIP and SO-8 interface-mount packages. Its 100fA max input current makes it ideal for high impedance sensors, low drift integrators, pH probe amplifiers, and ion gauge measurement. Its innovative input preserves its low bias current by allowing room for circuit board guard traces—even with the tiny SO-8 package. Key specs are: 100fA max bias current, 2mV max offset voltage, $0\mu\text{V}/^\circ\text{C}$ max drift, and $15\text{nV}/\sqrt{\text{Hz}}$ at 10kHz noise.

CIRCLE NO. 28

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New

$\pm 2\text{A}$, $\pm 35\text{V}$ Dual Power Operational Amplifier

OPA2544 is a dual, high-voltage, high-current operational amplifier suitable for driving high power loads. It packs two powerful amps in a single TO-3 package—saving board space and money. It provides output of up to 2A and its power supply range extends to $\pm 35\text{V}$. It's also ideal for programmable power supplies and automatic test equipment. Key specs are: 2A output current, $8\text{V}/\mu\text{s}$ slew rate, 50pA input bias current, internal current limit, and internal thermal shutdown protection. Available in an 8-pin metal hermetic TO-3 package.

CIRCLE NO. 31

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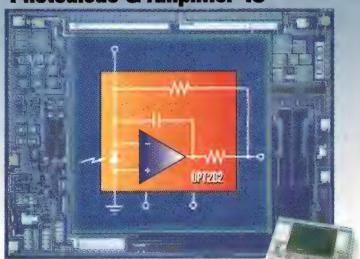
New Operational Amplifiers Brochure

A new eight-page brochure, *Operational Amplifiers*, features over twenty new op amps. It has selection guides on precision and high speed op amps along with complete descriptions, specifications, and applications info. Four pages of technical info highlight high speed amps, video amps, audio amps, precision amps, current-feedback amps, wide bandwidth amps, single power supply amps, precision FET amps, and switchable-input amps. Available from local sales representative.

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New Photodiode/Amplifier IC in "Optically Friendly" Package

OPT202 is now available in an innovative package—a new 5-pin SIP that mounts vertically for light sources entering the edge of a circuit board. It's ideal for many industrial applications including medical and laboratory instrumentation, position and proximity sensors, photographic analyzers, and smoke detectors. Key specs are: $1\text{M}\Omega$ feedback resistor, 2mV dark errors, $0.45\text{A}/\text{W}$ (650nm) responsivity, $400\mu\text{A}$ quiescent current, 0.05% nonlinearity, and ± 2.25 to $\pm 18\text{V}$ supply range.

GREEN PC BOARDS

through established pc-board processes and has been compared in detail with FR4 and the internationally accepted standard MIL-P-13949G (Table 1). Siemens has constructed a range of prototype pc-board assemblies and will introduce FRN material to its own electronic assembly lines during 1995.

Secondary savings tip balance

Naturally, the cost of FRN is a major concern, but according to Dr Wolfgang Rogler, thermosetting materials manager at Siemens, the overall penalty is not so severe. Rogler says that, most important, FRN is entirely compatible with established pc-board processes and equipment and involves users in no additional capital expense. The board material is around 10 to 20% more expensive than today's halogen-based alternative. Although the material is in full-scale production, this increase translates to less than 1% on a typical pc-board assembly.

Rogler says it's important for industry to recognize secondary cost savings that redress the balance. For example, pc-board production traditionally involves high levels of material waste due to cropping—up to 30%. The absence of halogens now opens up the prospect of recycling these waste products.

Also, the absence of corrosive and toxic effects dramatically reduces fire damage to surrounding equipment and the environment, leading to lower cleanup costs and, in turn, to lower insurance premiums.

FRN also has a higher glass transition temperature than FR4 and therefore exhibits greater structural stability at higher temperatures. This feature enables faster production using higher temperature flow soldering or implies fewer rejects due to board distortion at normal solder temperature. Greater stability also opens up the possibility of applications using thinner pc boards.

In the longer term, industry will have no choice but to follow a path to increasingly tighter environmental regulations. Eliminating halogens will be seen as a necessary step along that path—and one well worth paying for to secure a new level of environmental safety from electronic products.

ADOPTING A LIFE-CYCLE DESIGN MENTALITY

Creating products is a responsibility you accept with enthusiasm and relish. Destroying those same products is a responsibility you don't expect to carry and one you currently disregard.

Quite soon, though, that situation will change. You'll become just as responsible for your product's destruction as you now are for its creation. You will adopt a life-cycle design mentality (Ref 1). Your aim will be to minimize the

environmental impact of a design throughout its life—and during its eventual destruction. To do this, you'll need to design with components and materials and employ processes, such as easy disassembly, that prevent pollution and aid recycling. Eventually, your success in achieving these aims will become yet another measure of your product's quality.

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Design Guidance Manual," EPA/600/R-92/226, January 1993.

2. Philips Semiconductors, "Chemical content of semiconductor devices," 1993/94.

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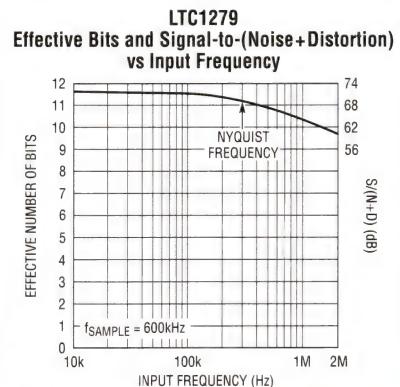
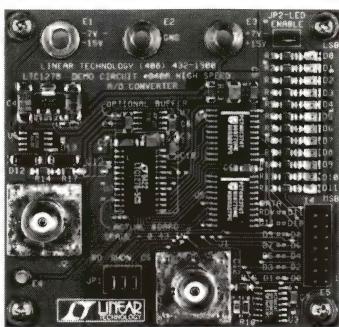
LINEAR SOLUTIONS
A/D CONVERTERS

Complete 12-Bit ADC Operates on Single 5V Supply at 600ksps

The LTC1279 is a high speed sampling ADC designed for demanding telecom and signal analysis applications. It has true 12-bit performance from DC to Nyquist.

Key Features are:

- 600ksps throughput
- 70dB S/(N+D) at Nyquist
- 60mW power dissipation and shutdown
- Complete ADC in small footprint
- Single 5V or \pm 5V supply



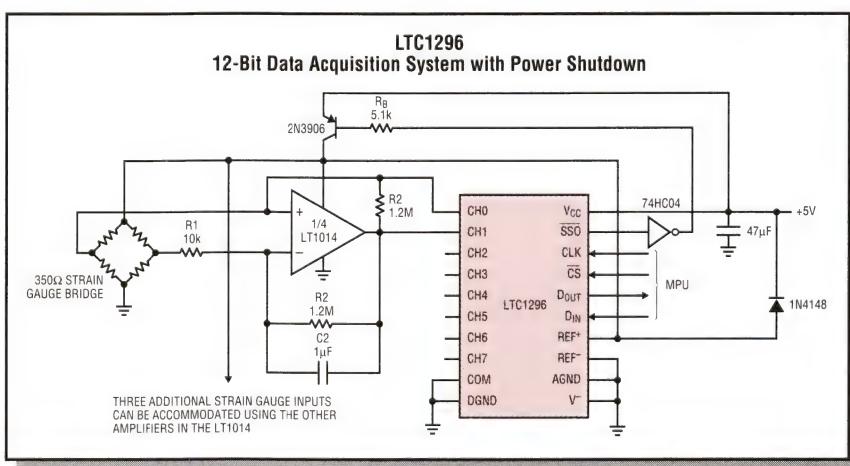
The LTC1279 contains a sample-and-hold, synchronized conversion clock, precision voltage reference and high speed, parallel interface to DSP and microprocessor ports. The LTC1279 also features an 8.5mW powerdown mode with instant wake-up for additional power savings and is available in narrow 24-pin DIP and SO packages.

Single Supply 8-Channel 12-Bit ADCs Have 10 μ A Shutdown

The LTC1296 is a 46ksps ADC designed to fit a wide variety of industrial process control equipment and multiplexed data acquisition systems.

Included on-chip are:

- Software programmable, 8-channel multiplexer
- Precision sample-and-hold
- Power shutdown mode with status pin
- Single 5V or \pm 5V supply operation



The multiplexer can be programmed for 8 single-ended or 4 differential inputs or combinations of both. The 3-wire serial interface is compatible with Microwire™, SPI and QSPI, and facilitates remote monitoring and isolated applications. Available in 20-pin DIP and SO packages. Pricing begins at \$8.23 in 1000-piece quantities, for 20-pin DIP.

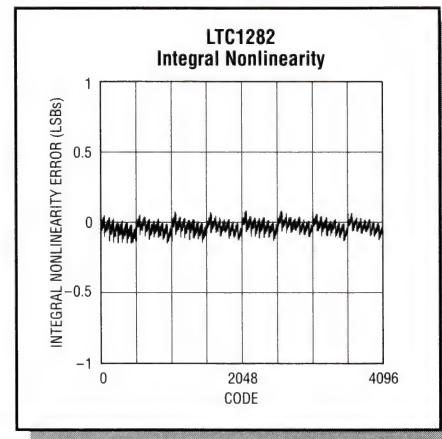
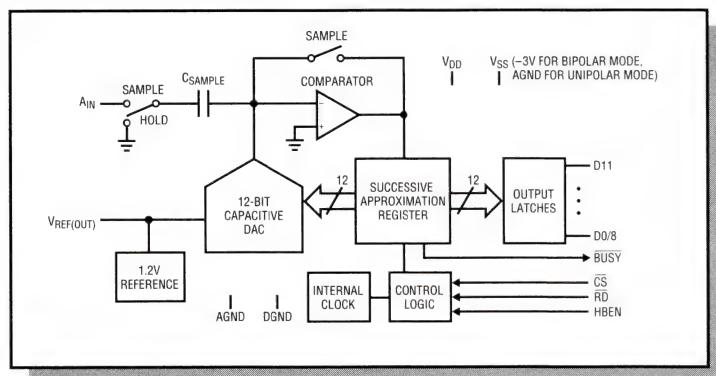
Complete High Speed 3V 12-Bit ADC for Portable Data Acquisition

Operating at 140ksps, the LTC1282 is a complete, high speed 12-bit ADC for 3V and ± 3 V supply applications that dissipates only 12mW. No missing codes and a $\pm 1/2$ LSB max INL combine to offer true 12-bit performance in a complete package. Dynamic performance is an outstanding 69dB S/(N+D) at Nyquist.

The LTC1282 comes complete with:

- Sample-and-hold
- Precision 25ppm/ $^{\circ}$ C voltage reference
- Easy to use, high speed parallel interface

Packaged in 24-pin DIP and SO, the LTC1282 fits a wide variety of portable and battery-powered applications including audio, spectrum analysis and telecommunications processing. Pricing for the LTC1282 begins at \$13.47 in 1000-piece quantities.

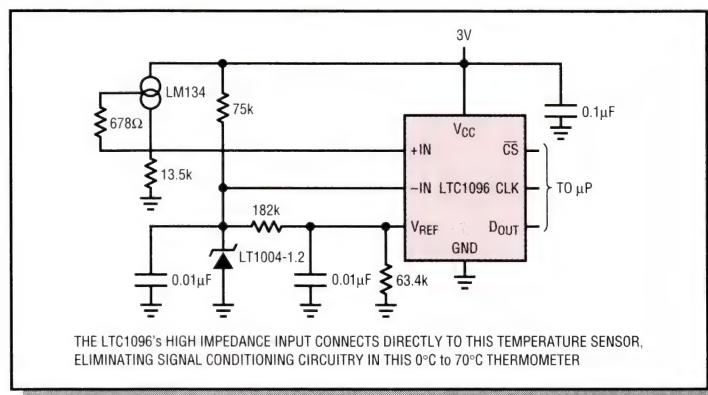
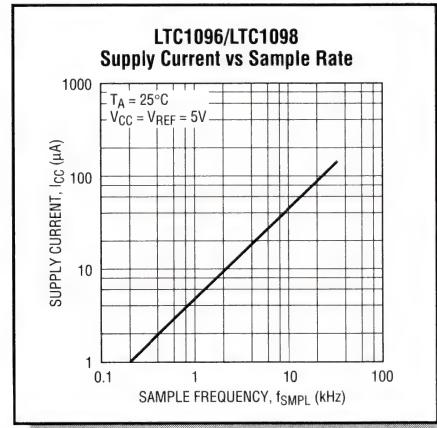


Low Cost 8-Pin SOIC, 8-Bit ADCs Auto-Shutdown to 1nA Supply Current

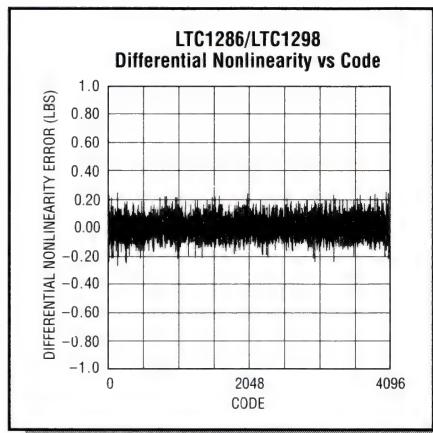
The LTC1096/LTC1098 are low cost 8-bit ADCs in 8-pin DIP and SO packages that operate from a single 3V to 9V supply. Operating current is a low 180 μ A max, and the devices automatically power down to 1nA between conversions, further increasing power

savings. The 3-wire serial I/O is Microwire, SPI and QSPI compatible and easily adapts to remote and isolated data acquisition.

The LTC1098 input has 2-channels while the LTC1096 features a differential input. Small size and low cost (\$2.82 in 1000-piece quantities) make the LTC1096/LTC1098 ideal for space conscious, power sensitive applications such as RSSI (Receive Signal Strength Indicator), battery monitoring and touch screen interface.



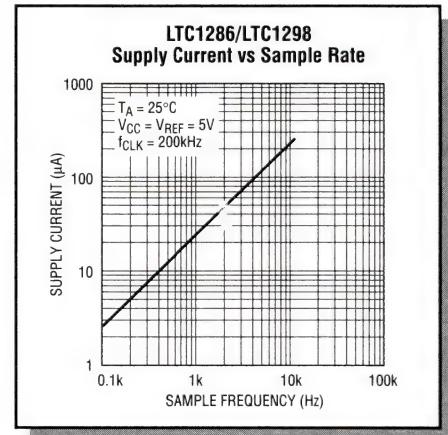
Micropower 12-Bit ADCs in SO-8 for Battery and Portable Systems



The LTC1286/LTC1298 are tiny 12-bit ADCs that draw 250 μ A from a single 5V supply when converting and automatically power down to 1nA between conversions. Packaged in 8-pin DIP and SOIC, the LTC1286 features a differential input while the LTC1298 input has 2 channels. Both devices have Microwire, SPI and QSPI compatible serial interfaces and easily accommodate isolated applications.

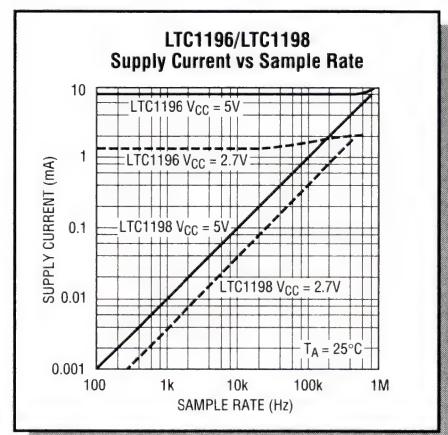
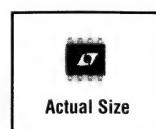
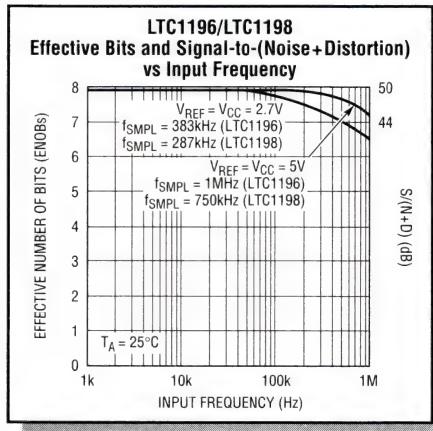
The LTC1285 and LTC1288 are pin compatible versions designed and specified for 3V supply applications.

Pricing begins at \$4.65 in 1000-piece quantities, perfect for high volume, space and power sensitive applications such as pen screen interface, remote data acquisition and battery monitoring and battery-powered portable instruments.



1MHz 8-Bit ADCs in SO-8 Save Power and Space

The LTC1196/LTC1198 are fast 8-bit ADCs that operate from a 3V or 5V single supply and convert 1MHz inputs to 7 Effective Bits. The LTC1196 has a differential input, and the 2-channel multiplexed LTC1198 automatically powers down to 1nA between conversions. Both devices are available in SO-8 packages and provide high speed 3-wire serial I/Os for RSSI, bar-code scanners and portable DSP. Low power (7mA typ), low cost (\$2.37 in 1000-piece quantities) and excellent dynamics make the LTC1196/LTC1198 ideal for demanding high frequency, power sensitive applications.



Sampling A/D Converters

Part	Resolution (Bits)	F _{SAMPLE} (ksps Max)	# of Inputs	V _{REF}	Data* I/O	V _{CC} (V)	P _{DISS**} (mW)	Features	Package†
LTC1096	8	33	1	Ext	Serial	2.7-9	0.6/0	Micropower SO-8 ADC	N8/S8
LTC1098	8	33	2	Ext	Serial	2.7-6	0.6/0	2-Channel LTC1096	N8/S8
LTC1196	8	1000	1	Ext	Serial	2.7-6	55	1Msps SO-8 ADC	N8/S8
LTC1198	8	750	2	Ext	Serial	2.7-6	55/0	2-Channel LTC1196	N8/S8
LTC1090	10	30	8	Ext	Serial	4-9	5	Low Power Multiplexed ADC	N20/S20
LTC1091	10	31	2	Ext	Serial	4-9	7.5	8-Pin 2-Channel ADC	N8
LTC1092	10	38	1	Ext	Serial	4-9	5	8-Pin 10-Bit ADC	N8
LTC1093	10	26	6	Ext	Serial	4-9	5	Low Power Multiplexed ADC	N16/S16
LTC1094	10	26	8	Ext	Serial	4-9	5	Low Power Multiplexed ADC	N20
LTC1095	10	26	6	+5.0	Serial	4-9	15	Complete 6-Channel ADC	N18
LTC1283	10	15	8	Ext	Serial	3-3.6	0.45	3V LTC1090	N20
LTC1286	12	12.5	1	Ext	Serial	4-9	1.25/0	Micropower SO-8 12-Bit ADC	N8/S8
LTC1298	12	11.1	2	Ext	Serial	4-6	1.7/0	2-Channel LTC1286	N8/S8
LTC1290	12	50	8	Ext	Serial	4-6	30/0.05	8-Channel ADC	N20/S20
LTC1291	12	54	2	Ext	Serial	4-6	30/0.05	8-Pin 2-Channel ADC	N8
LTC1292	12	60	1	Ext	Serial	4-6	30	8-Pin 12-Bit ADC	N8
LTC1293	12	46	6	Ext	Serial	4-6	30/0.05	6-Channel ADC	N16
LTC1294	12	46	8	Ext	Serial	4-6	30/0.05	8-Channel ADC	N20/S20
LTC1296	12	46	8	Ext	Serial	4-6	30/0.05	LTC1294 w/ Shutdown Output	N20/S20
LTC1297	12	50	1	Ext	Serial	4-6	30/0.05	LTC1292 w/ Auto-Shutdown	N8
LTC1285	12	7.5	1	Ext	Serial	2.7-6	0.48/0	3V LTC1286	N8/S8
LTC1288	12	6.6	2	Ext	Serial	2.7-6	0.63/0	3V LTC1298	N8/S8
LTC1287	12	30	1	Ext	Serial	2.7-6	3	3V LTC1292	N8
LTC1289	12	25	8	Ext	Serial	2.7-6	3/0.03	3V LTC1290	N20/S20
LTC1272-8	12	100	1	2.42	µP 8 or 12	+5	75	Sampling AD7572-12	N24/S24
LTC1272-3	12	250	1	2.42	µP 8 or 12	+5	75	Sampling AD7572 A-3	N24/S24
LTC1273	12	300	1	2.42	µP 8 or 12	+5	75	5V High Speed ADC w/Ref	N24/S24
LTC1275	12	300	1	2.42	µP 8 or 12	±5	75	High Speed ADC w/Ref	N24/S24
LTC1276	12	300	1	2.42	µP 8 or 12	±5	75	High Speed ADC w/Ref	N24/S24
LTC1278-4	12	400	1	2.42	µP 12	5/±5	75/5	Sampling ADC w/ Shutdown	N24/S24
LTC1278-5	12	500	1	2.42	µP 12	5/±5	75/5	Sampling ADC w/ Shutdown	N24/S24
LTC1279	12	600	1	2.42	µP 12	5/±5	75/5	Sampling ADC w/ Shutdown	N24/S24
LTC1282	12	140	1	1.20	µP 8 or 12	3/±3	12	3V Sampling ADC	N24/S24

* Serial I/O is Microwire, SPI and QSPI compatible

** Power dissipation is listed in the Active and Shutdown modes

† N8 = 8-pin DIP S8 = 8-pin SOIC

N16 = 16-pin DIP S16 = 16-pin SOIC

N18 = 18-pin DIP S20 = 20-pin SOIC

N20 = 20-pin DIP S24 = 24-pin SOIC

N24 = 24-pin DIP



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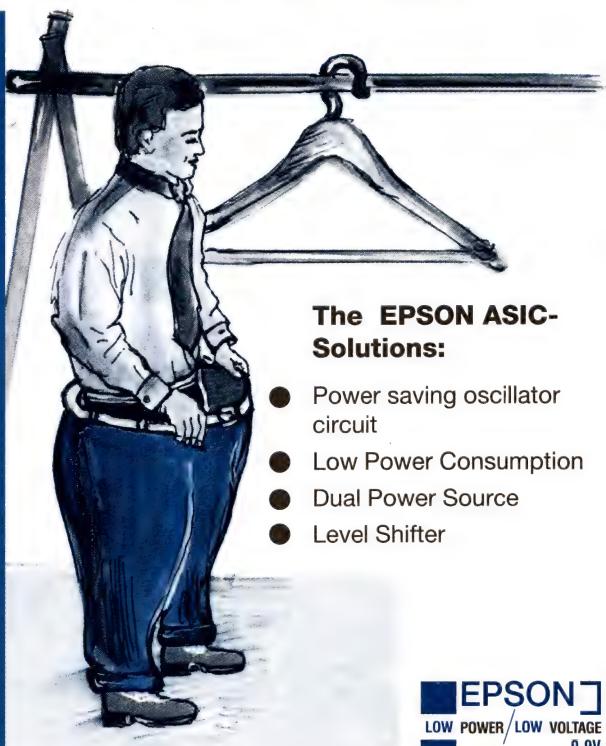
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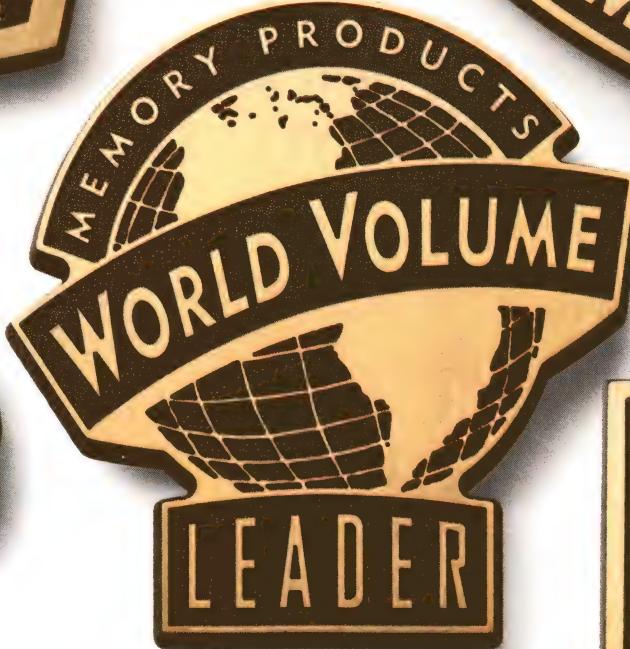
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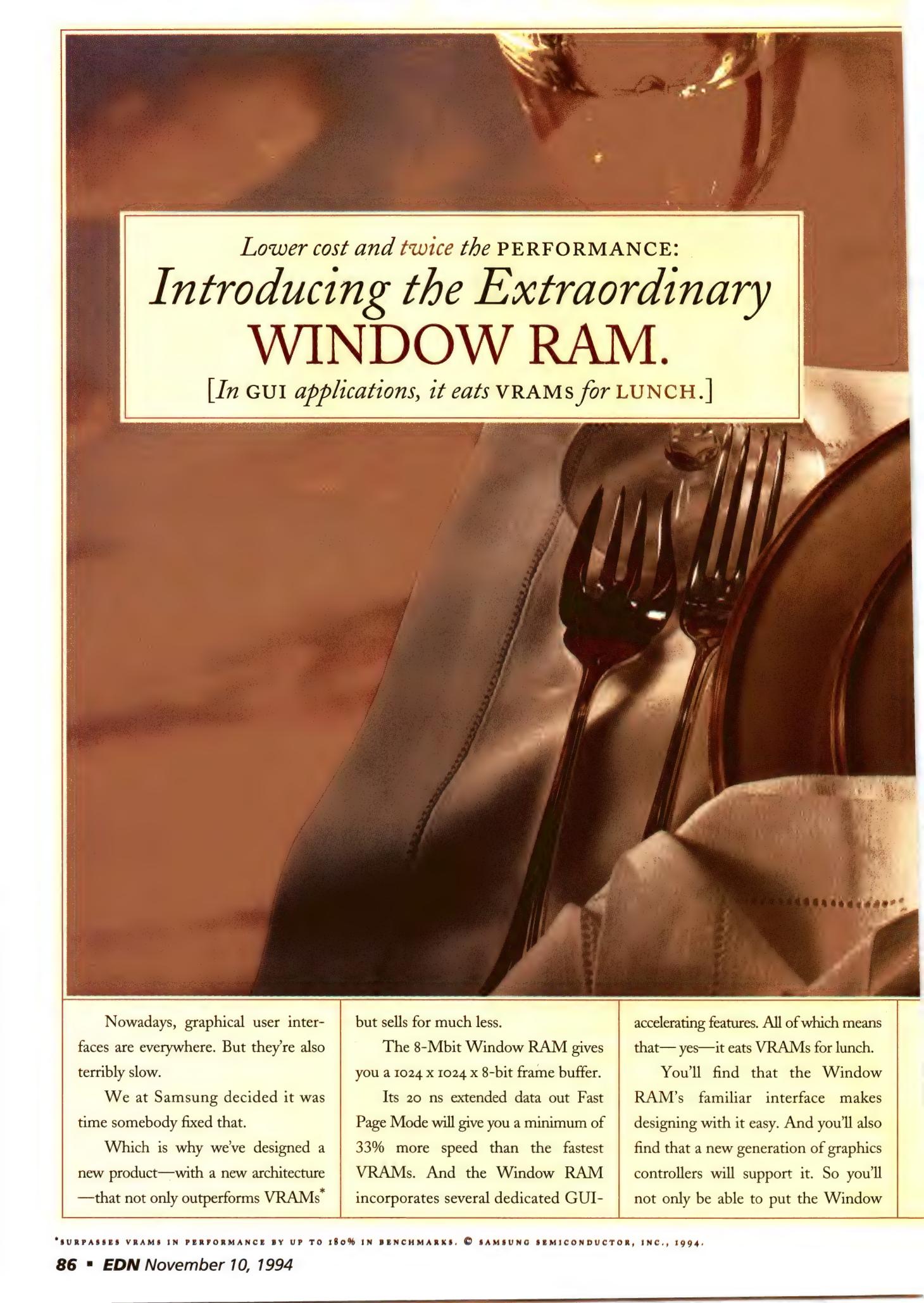
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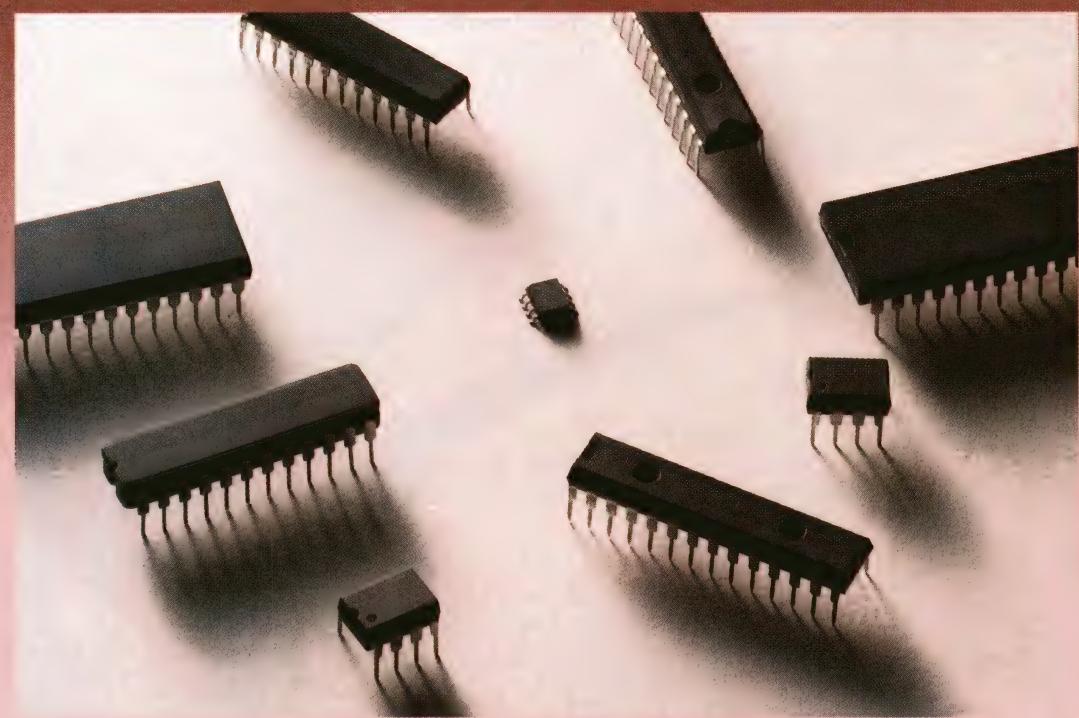
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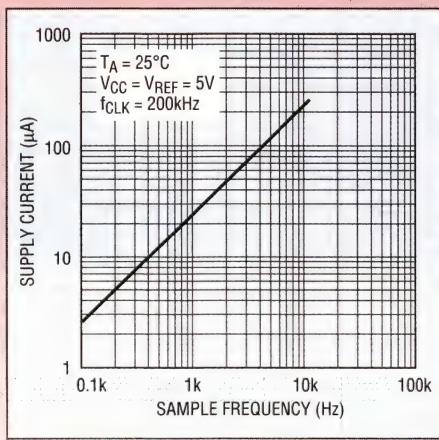


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LTC1298 draws 340 μ A at 11.1ksps. Power drain drops even more in auto-shutdown to 20 μ A at 1ksps, and at idle it plunges to 1 nanoamp!

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Digital tachometer avoids analog vices

TAN VAN NGUYEN, IBM SSD DIVISION, SAN JOSE, CA

The digital tachometer in Fig 1a is a component of the digital seek servo loop in Fig 1b. The loop produces an error signal that causes a motor to follow a sophisticated velocity profile (Fig 2). Although you could use an analog tachometer, the digital one costs less, performs better, is less sensitive to temperature, and implements easier in a custom IC.

My design's tachometer controls the actuator for the heads of an optical-disk drive. But the principle also applies to other motor-control applications.

Upon receiving a start command, the actuators accelerate to a desired speed and follow the specified velocity profile until they reach their destination.

As the actuators move across the tracks, they generate two pulses for each track they cross. The circuit samples these pulses at different rates depending on how close the actuators are to their final destination. Table 1 lists the specific sampling rates.

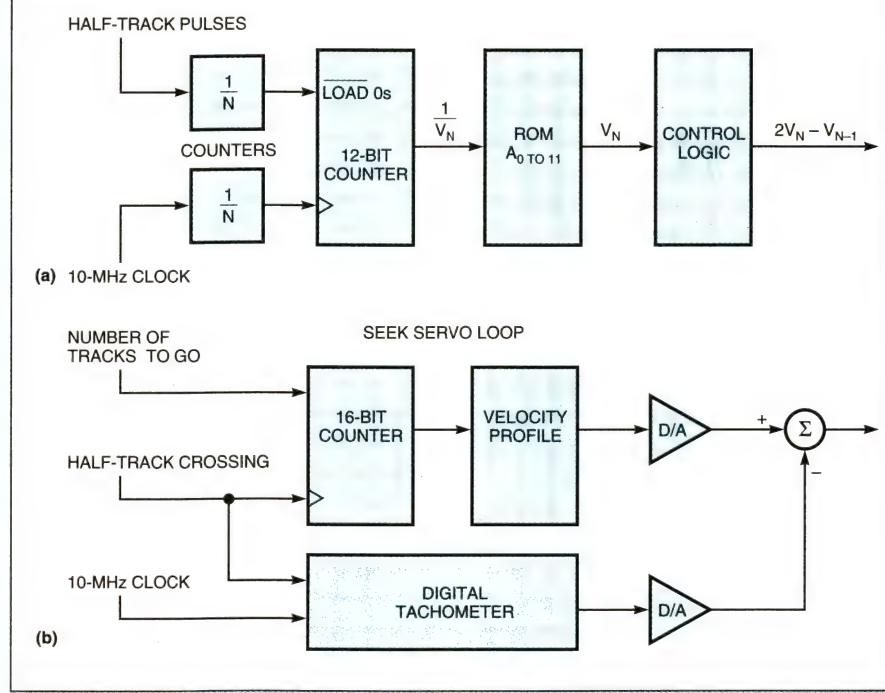
A 10-MHz clock provides the fundamental sample rate; but the actual sample rates vary. Therefore, the circuit must divide the time between samples by that same sample rate to obtain the correct time interval for each pulse. Otherwise, the output A/D converters would not produce a properly scaled error signal.

In Fig 1, two 4-bit counters divide the input-pulse signal and the 10-MHz clock by the appropriate divisor from Table 1. The overflow output of the input-pulse's 4-bit counter loads all zeros into the 12-bit counter. The 4-bit counter's overflow output clocks the 12-bit counter. Thus, the output of the 12-bit counter always represents the time required for a single input pulse, regardless of the sample rate.

A 4-kbyte PROM converts the output of the 12-bit counter to velocity. The circuit in Fig 1b compares the actual velocity with the desired velocity, producing an error signal for the actuator. (DI #1612)

EDN

FIGURE 1



The digital tachometer in (a) cleverly adjusts its sampling rate to match varying rates of input pulses. The sampling rate varies as the actuator being controlled approaches its target (Table 1). The circuit in (b) compares the tachometer's output with the actuator's desired speed.

TABLE 1—DISTANCE TO DESTINATION VS SAMPLING RATE

Number of tracks to go	Pulse-sampling rate (2 pulses/track)
<425	16
425 to 153	8
152 to 68	4
67 to 7	2
6 to 0	1

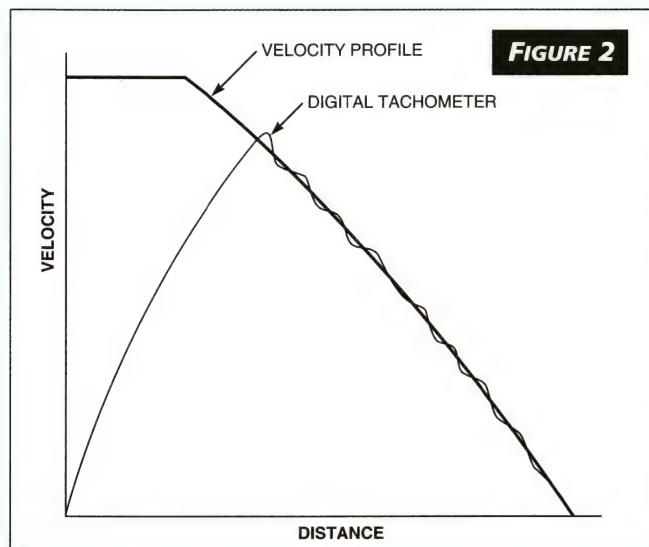


FIGURE 2

After accelerating an actuator, the digital tachometer tracks the actuator's speed. This tracking produces an error signal, so the actuator follows a desired velocity profile as it homes in on its destination.

To Vote For This Design, Circle No. 374

Software configures IBM PC interrupts

SAID JACKSON, CONSULTANT, HAMBURG, GERMANY

Anyone who has installed an expansion card in an IBM PC-AT expansion slot has dealt with interrupt conflicts. Often, despite the manufacturer's claims of "plug-and-play" compatibility, inserting a simple I/O card turns a fully functional computer into a brain-dead piece of equipment. Interrupt assignments and the possible resulting conflicts usually cause this pernicious problem.

Under software control, the circuit in Fig 1 can dynamically assign an interrupt-channel to an I/O card based on available channels. (The new PCI bus from Intel uses the same methodology.)

The 8-bit ISA bus provides six external-interrupt lines for expansion cards. Because the assignment of these interrupts is not standardized, more than one card may come from its factory set to the same interrupt line.

Now, multiple cards that use the same interrupt line are not necessarily bad. The ISA bus permits multiple cards assigned to the same interrupt. In fact, serial-I/O cards frequently use this scheme because PCs come hardwired with

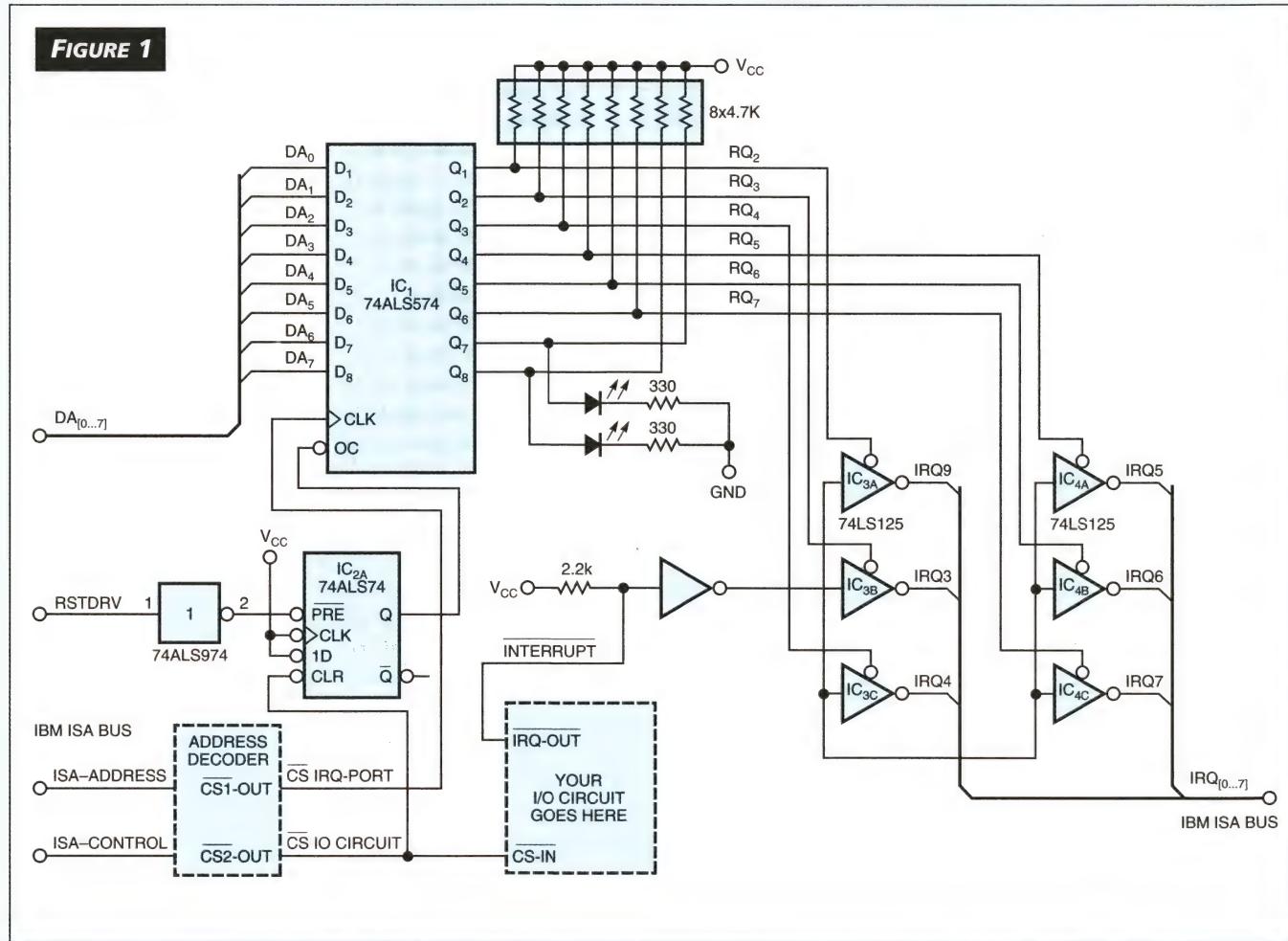
COM1 sharing an interrupt line with COM3 and COM2 with COM4.

But, in some cases, the interrupt-handler software cannot resolve such a conflict and the system crashes. Instead of forcing the user to troubleshoot the system by tediously changing jumper settings, the circuit allows the software to reconfigure the I/O board. Today's users demand such comfort and find any other setup highly anachronistic.

The heart of the circuit is an 8-bit register, IC_1 , that stores the selected interrupt for the card. The software selects an interrupt line by writing a zero into the corresponding register bit. The software must first set all unselected interrupt bits to a logic 1. You can use the two leftover most-significant bits as general-purpose output bits. In our case, we used the bits to drive two status LEDs.

Your main concern is the circuit's cold-start behavior. The circuit must deactivate all interrupts upon power-up because the status of the register is undefined. The PC's reset-driver signal presets flip-flop IC_{2A} at power-up and disables IC_1 's out-

FIGURE 1



A simple setup program can dynamically assign an interrupt-channel to an IBM PC's I/O card, based on currently available channels.

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CIRCLE NO. 115

puts. The resistor pullups ensure that the tri-state interrupt line-drivers of IC_3 and IC_4 are inactive and can't assert any interrupts.

At this time, the interrupt driver can find a free interrupt line by checking the CPU's interrupt-vector table. After finding an unused interrupt, the software activates the add-in board's interrupt line by writing a logic 0 into its register. The system is active but not triggered.

The software initializes the board's I/O-port controller. The first chip-select of the I/O controller resets flip-flop IC_{2A} .

In turn, this action activates the output of the interrupt register IC_1 . Now the controller's interrupt requests can propagate through the 74LS125 drivers to the CPU. Pushing IC_1 deselects all interrupts on the board, and the system is clear again.

This circuit works in both 8- and 16-bit IBM expansion slots. To use all available interrupts you need an IBM-AT, a second register, and some more 74LS125 drivers. (DI #1614)

EDN

To Vote For This Design, Circle No. 375

Oscillator keeps THD below 1 ppm

JEFF SMITH, ANALOG DEVICES, WILMINGTON, MA

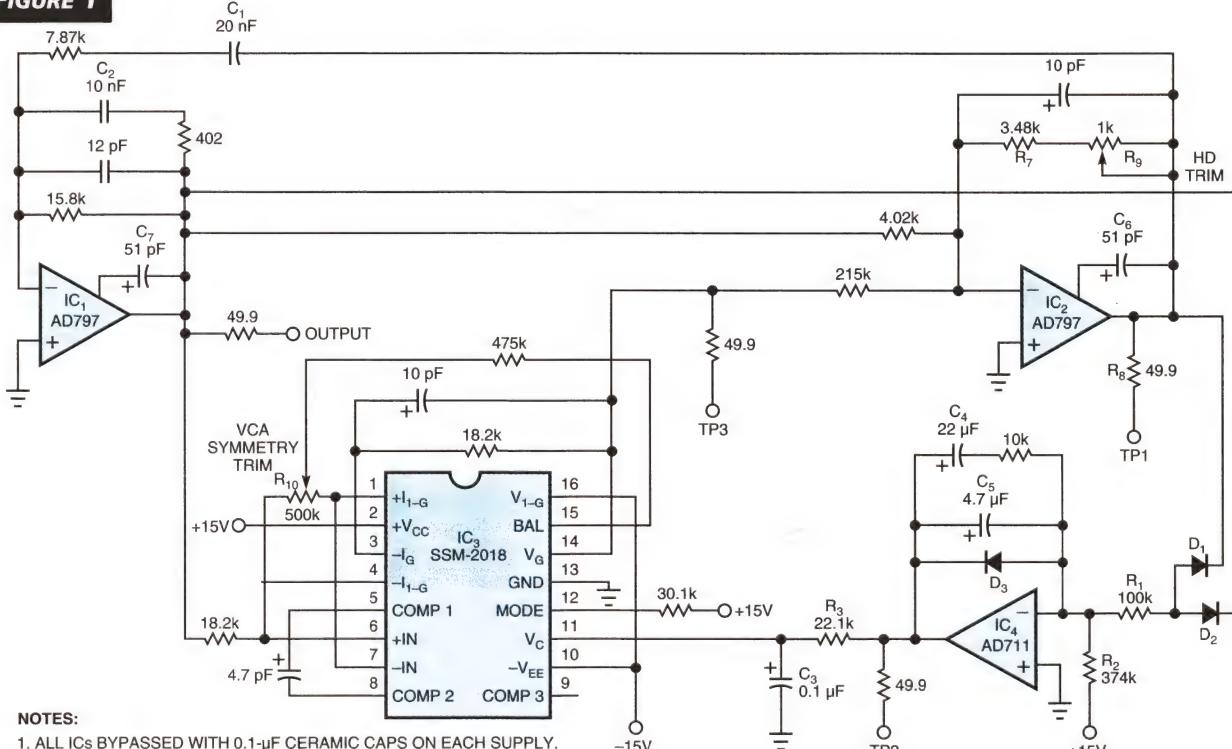
The Wien-bridge sine-wave oscillator uses a light bulb to stabilize its amplitude. The circuit in Fig 1 doesn't have a light bulb; it sports several enhancements that lower its distortion and generate a test signal pure enough for testing modern op amps and high-resolution A/D converters.

IC_1 and associated components form the Wien-bridge and function as a bandpass filter. IC_1 's output goes to the voltage-

controlled amplifier (VCA), IC_3 . IC_3 acts as a "smart resistor" whose value the circuit continuously adjusts via IC_4 . IC_2 adds the outputs of IC_1 and the VCA and feeds the result into the bridge. These two op-amp inverters eliminate any common-mode signal that might limit performance.

The circuit's AGC loop begins with diodes D_1 and D_2 . These diodes half-wave rectify the outputs of IC_1 and IC_2 .

FIGURE 1

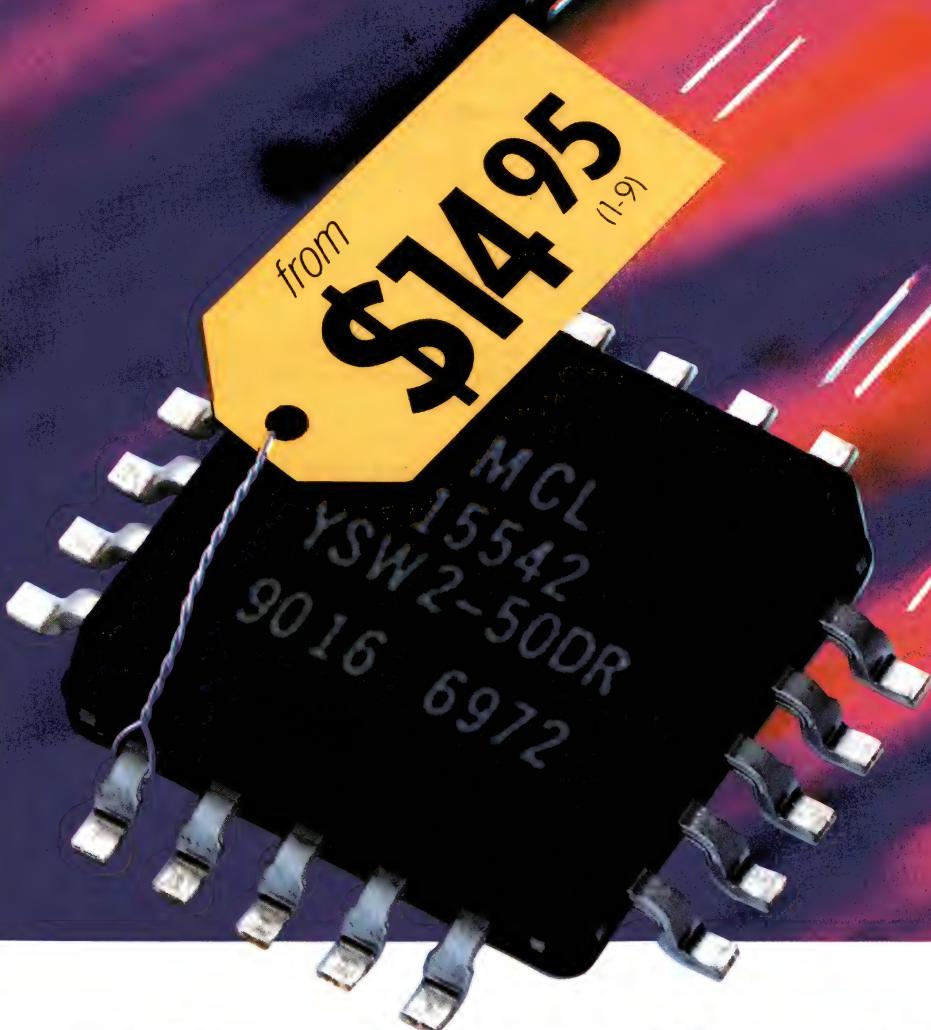


NOTES:

1. ALL ICs BYPASSED WITH 0.1- μ F CERAMIC CAPS ON EACH SUPPLY.
2. ALL ICs USE ± 15 V SUPPLIES.
3. ALL DIODES ARE 1N4148.
4. C_1 AND C_2 ARE POLYSTYRENE, OUTSIDE FOIL AS SHOWN.
5. C_3 THROUGH C_8 ARE SILVER MICA.
6. R_9 IS A MULTITURN TRIMMING POTENIOMETER.

This Wien-bridge sine-wave oscillator sports several enhancements that lower its distortion and generate a test signal pure enough for testing modern op amps and high-resolution A/D converters.

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Ins. Loss (dB)	1.1 1.4 1.9			0.9 1.3 1.4		
Isolation (dB)	42 31 20			50 40 28		
1dB Comp. (dBm)	18 20 22.5			20 20 24		
RF Input (max dBm)	— 20 —			22 22 26		
VSWR "on"	1.25 1.35 1.5			1.4 1.4 1.4		
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These outputs are 180° out of phase; so IC_4 sees a full-wave rectified signal through R_1 that is proportional to the output signal's amplitude.

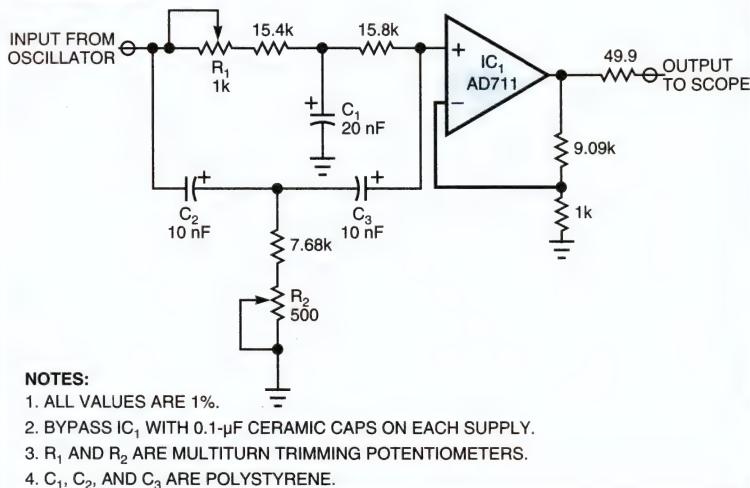
Integrator IC_4 compares the average value of the rectified current to a constant current through R_2 . Any imbalance in these currents causes IC_4 to output a correction signal, changing the gain of VCA IC_3 . The VCA's gain adjusts the oscillation's amplitude until IC_4 's input currents are equal. R_3 and C_3 further filter the correction signal to remove harmonic components that would manifest themselves as distortion at the circuit's output. D_3 minimizes damage to C_4 and C_7 in the event of reverse polarization.

The ac performance of C_1 and C_2 is critical to this design. I recommend polystyrene or polypropylene film types; and make sure you connect the outside plate as Fig 1 indicates. Mylar capacitors can degrade the circuit's performance by 6 dB. C_5 and C_6 are peculiar to IC_1 and IC_2 . They eliminate distortion arising from V_{BE} nonlinearities in the op amps' output stages.

The large ratio of output signal to distortion and noise floor makes verifying the performance of this circuit with standard test equipment difficult. Therefore, I used the tunable, buffered-output, twin-T filter in Fig 2 to reduce the fundamental (1 kHz) in the output by 70 dB. Spectral analysis of the filter's output permits calculation of THD.

When properly tuned, the filter reduces the second and third harmonics by about 10 and 5 dB, respectively. Harmonic-distortion calculations must take this reduction into account. Harmonic-distortion calculations must factor in the gain of IC_1 (Fig 2). Be sure to use the same high-performance capacitors used for C_1 and C_2 in Fig 1 for C_1 , C_2 , and C_3 in Fig 2.

FIGURE 2



Because the large ratio of output signal to distortion and noise floor makes verifying the performance of the circuit in Fig 1 difficult, you need this tunable, buffered-output, twin-T filter, which reduces the fundamental (1 kHz) in the output by 70 dB.

To tune the filter:

- Adjust R_9 so that R_7 shorts to R_8 .
- Monitor TP3 on an oscilloscope and adjust R_{27} for a visually undistorted sine wave.
- Using the filter, adjust R_{10} for a minimum second-harmonic distortion at TP3.

Note: You may need to make small adjustments to R_9 for successful power up. (DI #1617)

EDN

To Vote For This Design, Circle No. 376

Digital pot corrects for system drift

MARK RUTLEDGE, XICOR INC, MILPITAS, CA

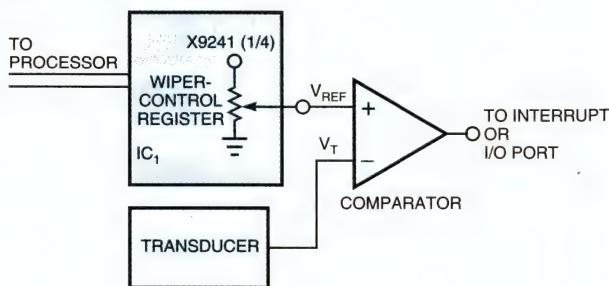
The circuit in Fig 1 looks simple but usually comes as a revelation to designers. Under control of the system's μ P, the digital potentiometer, IC_1 , becomes a variable set-point reference that can adapt to the long-term drift of the variable measured. The digital potentiometer replaces schemes involving A/D and D/A converters (see "Autocalibrator nulls dc offsets," EDN, June 9, 1994, pg 139, and "Infinite-hold circuit zeros out long-term drift," EDN, March 3, 1994, pg 90).

Depending on how you configure IC_1 , its resolution will be 0.79, 0.53, or 0.40%. Cascading two devices yields 0.024% resolution. Internal EEPROM registers store the digital potentiometer's "wiper" position, allowing the system μ P to determine the current set point, even after power outages. (DI #1615)

EDN

To Vote For This Design, Circle No. 377

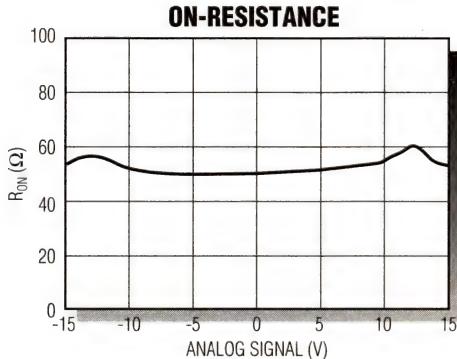
FIGURE 1



Under control of the system's μ P, IC_1 becomes a variable set-point reference that can adapt to long-term drift of the variable.

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On-Resistance Flatness (Ω)	7 (max)	Not Specified	7	Not Specified
Off-Leakage at 85°C (nA)	2.5 (max)	5	2.5	5
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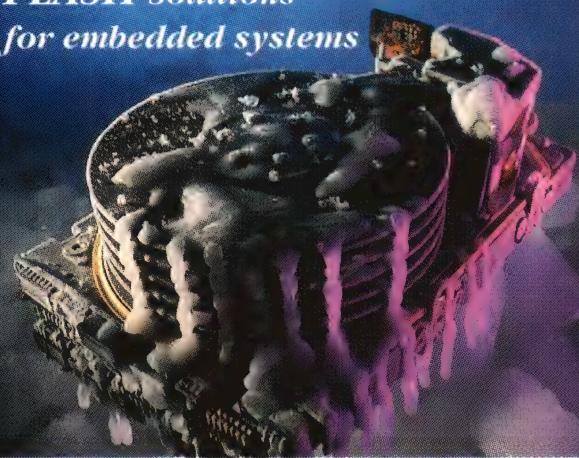
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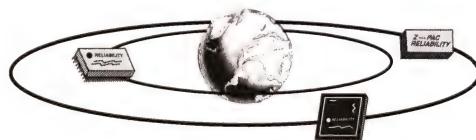
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CIRCLE NO. 104

**Disassembler takes on
8-bit Intel µPs and µCs**

**K V RAMAKRISHNAN, DRDO, NPOL
COCHIN, KERALA, INDIA**

The disassembler and documentation in the ZIPfile attached to EDN BBS /DI_SIG #1624 handles the object code for 8048, 8051, 8080, and 8085 family processors.

To Vote For This Design, Circle No. 378

µC routines clear up errors

**MIKA MAASPURO, KIRSTINMAKI
ESPoo, FINLAND**

The ZIPfile attached to EDN BBS /DI_SIG #1619 contains executable programs and source code for programs that allow you to program MC68HC11 microcontrollers via an RS-232C connection to your PC. The programs replace obsolete, error-laden programs published in an applications note.

To Vote For This Design, Circle No. 379

**Spice filters allow experimenting
without designing actual circuits**

**GEORGE ELLIS, KOLLMORGEN
RADFORD, VA**

This ZIPfile attached to EDN BBS /DI_SIG #1620 contains some popular filters you can use with Spice models. Specified in terms of frequency and damping factor, the filter models allow you to experiment without having to design working filters.

To Vote For This Design, Circle No. 380

**C program simulates
industrial temperature system**

**JYOTI VANDANA, WORLD FRIENDS DESIGN GROUP
KALPAKKAM, TAMILNADU, INDIA**

The program in the ZIPfile attached to EDN BBS /DI_SIG #1621, written in Borland C, simulates industrial-temperature-data display and control. It displays four independent channels simultaneously.

To Vote For This Design, Circle No. 381

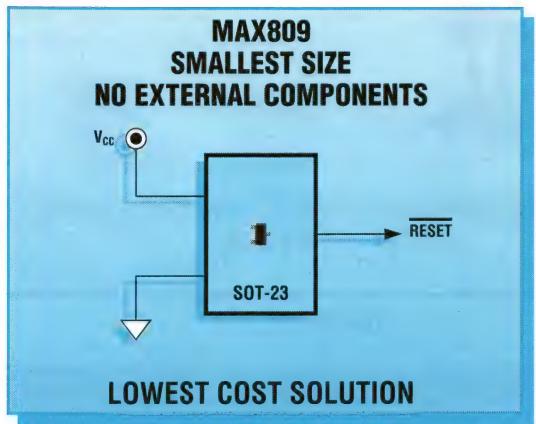
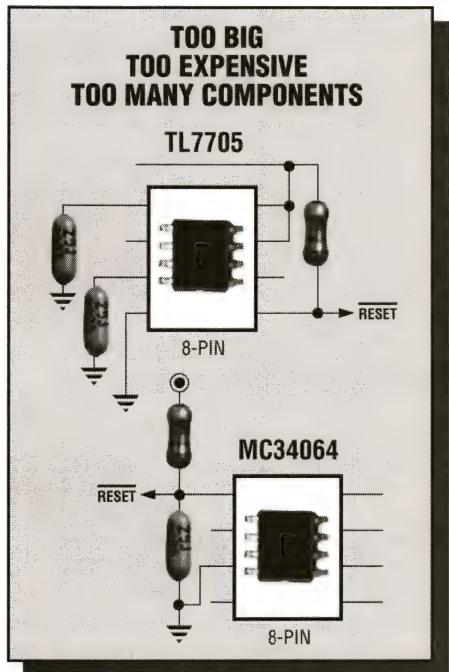
Correction

"Passive components cancel phase errors," (EDN, June 9, 1994, pg 147) contains errors. The symbol for the load should be r , not R . The label for the inductor in the left-bottom branch of the bridge should be L , not L_1 . The expression $F_o/2$ in the seventh line from the bottom of the first column of text should be $f_o/2$. Finally, omit the + signs from the capacitors; they are not electrolytics.

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DESIGN NOTES

High Efficiency Power Sources for PentiumTM Processors

Design Note 90

Craig Varga

In many applications, particularly portable computers, the efficiency of power conversion is critical both from the standpoint of battery life and thermal management. Desktop machines may also benefit from higher efficiency, particularly a "green PC." While linear regulators can offer low cost and high performance solutions, they can only offer 67% efficiency in 5V to 3.3V applications. Switching regulators are more efficient and minimize or even eliminate the need for heat sinks at a higher cost for the components. Efficiencies around 90% are routinely obtained with Linear Technology's best regulator designs (see Figure 2). The LTC1148 based circuit (Figure 1) meets the requirements of the P54-VR specification for output voltage transient response with the indicated decoupling network.

Selection of Input Source

Several options exist as to where to derive raw power for the regulator input. In most desktop systems a large amount of 5V power is available. Also, there is usually a reasonable source of 12V at hand. The 5V supply will most likely have the highest power output capability since it is called upon to power the bulk of the system logic. This logic can be sensitive to voltage changes outside of $\pm 5\%$.

When the processor draws large transient currents, the 5V supply will be perturbed. In all "buck" type switching regulators there is an inductor in the path between the raw input supply and the load. This has the effect of limiting the rise time of the input currents and minimizing the disturbance to the 5V supply. However, the typical cheap off-line "brick" supply has terrible transient response, and the 5V

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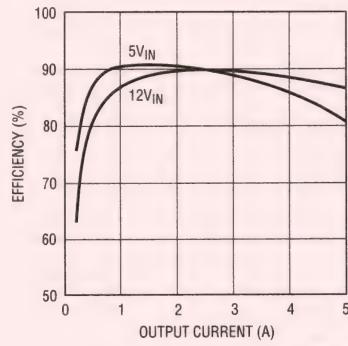
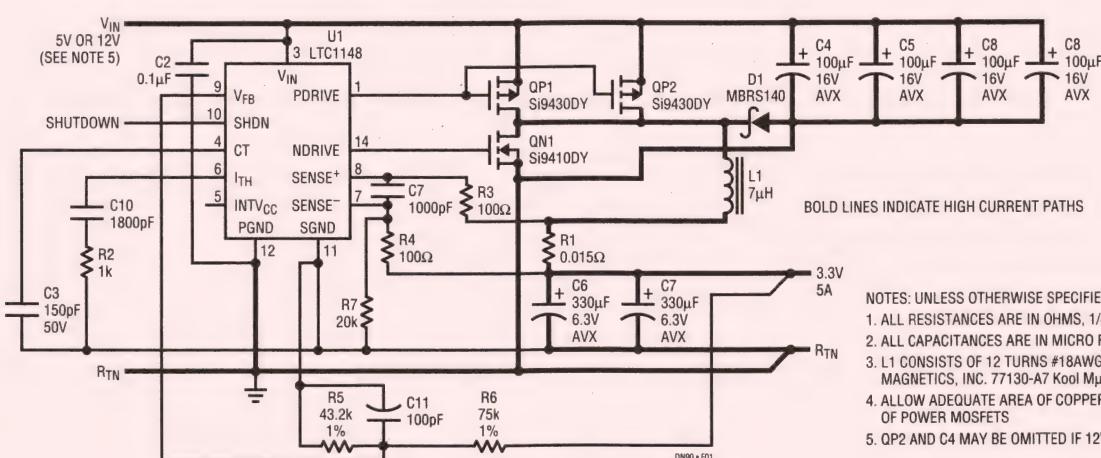


Figure 2. Efficiency vs Load



NOTES: UNLESS OTHERWISE SPECIFIED
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 2. ALL CAPACITANCES ARE IN MICRO FARADS, 50V, 10%
 3. L1 CONSISTS OF 12 TURNS #18AWG WIRE ON A MAGNETICS, INC. 77130-A7 Kool Mu[®] CORE
 4. ALLOW ADEQUATE AREA OF COPPER FOR COOLING OF POWER MOSFETS
 5. QP2 AND C4 MAY BE OMITTED IF 12V INPUT IS USED

Figure 1.

supply may still be disturbed enough to cause logic problems. This is especially true as the load currents rise to the levels expected in multiprocessor systems.

If this is the case, using the 12V supply may prove advantageous. Since the 12V supply is not directly regulated, nothing that is terribly sensitive to voltage level is normally powered off the 12V bus. Moreover, with switching regulators, as a first order approximation, as the supply voltage rises the input current drops. As such, even though the input power is nominally the same whether running from a 5V or 12V supply, the current requirement is much lower if 12V is utilized for the input source.

The downside of 12V operation is lower light load efficiency than 5V operation. The efficiency with a 5V input powering a 3.3V switcher is likely to be several percentage points better than at 12V due to a reduction in switching losses. Every situation is somewhat different and a thorough analysis of the trade-offs must be undertaken to optimize the design. The schematic shown in Figure 1 offers the option to run from several supply choices. Each circuit was optimized for the specified input voltage, but will function well over a fairly wide range of supply voltages.

Transient Response Considerations

As with a linear regulator, the first several microseconds of a transient are out of the hands of the regulator and dropped squarely in the lap of the decoupling capacitor network. In the case of the switcher, the ultimate response of the regulator will be quite slow compared to a linear regulator. In the circuits shown, the approximate time required to ramp the regulator current to equal the high load condition is 11 μ s, about 2.4 times that of an LT1585 high speed linear regulator in the same application. This means in layman's terms, that the LT1585 linear regulator requires less bulk capacitance than the LTC1148 switcher solution.

Circuit Operation

Figure 1 is a schematic of the two regulators. For the 12V input, omit QP2 and C4. The design is a standard synchronous buck regulator that is discussed in detail in several Linear Technology Application Notes as well as the LTC1148 data sheet. Since the required output voltage is not the standard 3.3V, which is available factory set, an adjustable regulator is used. R5 and R6 set the output voltage to the desired level, in this case 3.38V. R7 is used to inhibit Burst Mode™ operation at light loads. If the system were permitted to operate in Burst Mode, the

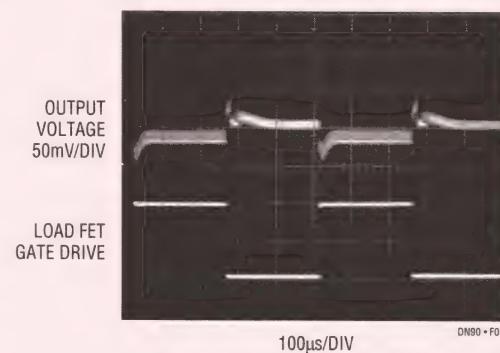
output voltage would rise by about 50mV at low load currents. If added low load efficiency is desired and the slightly higher low load output voltage can be tolerated, this resistor can be omitted.

To meet the transient requirements of the P54-VR, a fairly large amount of capacitance is needed beyond what is required to make the regulator function correctly. A viable decoupling scheme is to use 10 each, 1 μ F surface mount ceramics and 7 each, 220 μ F, 10V surface mount tantalums at the processor socket. In addition to the socket decoupling, two pieces of a 330 μ F, 6.3V surface mount tantalums are required at the power supply.

The input capacitors were selected for their ability to handle the input ripple current. At a 5A load current this is a little over 4A with a 5V input and 2.6A for a 12V input. The capacitors are rated at slightly over 1A each at 85°C. If the input can be switched on very rapidly, the input capacitor voltage rating should be at least two times the supply voltage to prevent dV/dt failures.

By running the operating frequency at 150kHz, the small inductor used is sufficient. Also, since the design is synchronous, the ripple current may be permitted to get quite high without causing any problems for the regulator control loop. This would not be true in a non-synchronous design. A major advantage of high ripple current is the regulator's ability to ramp output current rapidly. The rate of rise of output current is directly proportional to input/output differential and inversely proportional to the inductor value. Using a small inductor aids in achieving fast response to transients.

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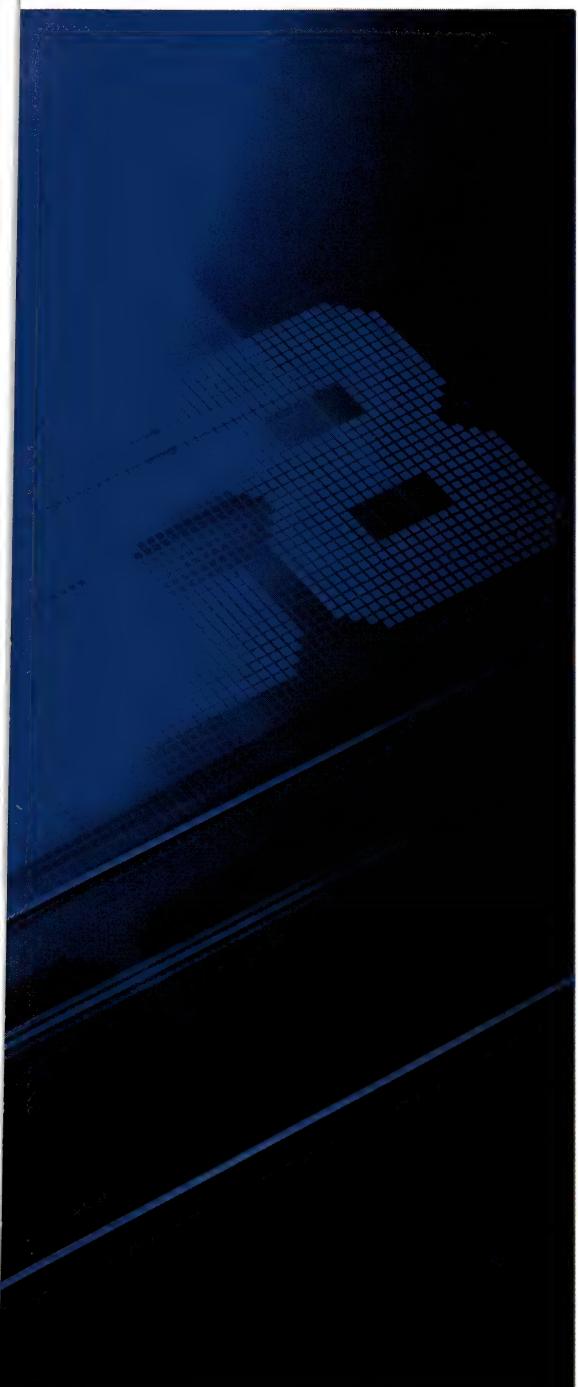
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Combine software tools to devise your own FPGA-verification environment

LEO BREDEHOFT, NETRIX TELCOM SYSTEMS, BOULDER, CO

Many characteristics of FPGAs (field-programmable gate arrays) make preprototype design verification necessary. FPGA designs frequently contain buried states that you cannot probe in a prototype. Modification to FPGA's designs can prove costly. Place-and-route software that runs for some FPGAs can require as long as a day to complete. So, even for reprogrammable FPGAs, preprototype design verification can save development time.

To raise your level of confidence in the buried logic in an FPGA's design, you can simulate the design to verify it before ever fabricating pc boards. Here's how: You must first build a programmatic environment around your design. You then exercise your design by forcing all of its state sequences and generating as many asynchronous stimuli for the design as possible. Design verification can increase your chances of having a functional device when you initially install it in a prototype.

Development environment

Fig 1 shows the FPGA development environment best suited to the kind of design verification described in this article. You code most of your design environment in an HDL (hardware-description language) to keep your development time short and produce maintainable source code. Because of space and performance requirements, you draw gate-level schematics wherever necessary.

Both design methods produce

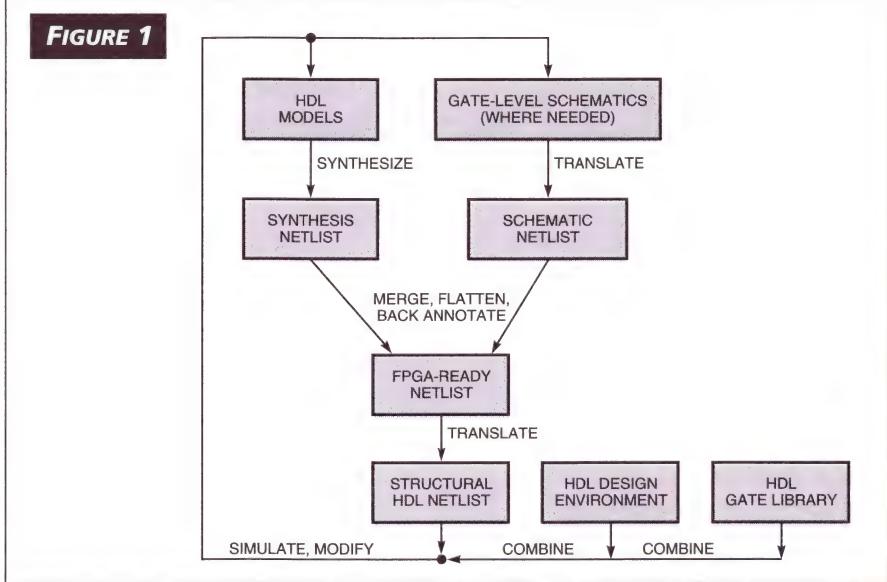
Armed with working knowledge of a modeling language such as VHDL and a simulator, you can verify an FPGA's design and reduce prototype-debugging time. This article discusses verifying FPGA designs and provides concrete examples demonstrating this practical, low-cost approach.

netlists. You merge the resulting netlists and "back-annotate" them using tools from the FPGA vendor. A simple reformatting utility then converts the back-annotated, merged netlist into a flat, structural HDL model that is ready for simulation. You can use reformatting utilities to perform this last conversion. The reformatting is not likely

to insert undetectable errors.

The last step combines your design's model with a set of HDL models of your design's operational environment and gates from a library for the gates invoked in your FPGA's netlist. The resulting total model allows you to simulate and iterate your design. This collection of models, in conjunction with the accompanying scripts and conversion programs, constitute the design-verification environment.

FIGURE 1



This FPGA development environment suits design verification. Most of the design environment is in an HDL; where necessary, you draw gate-level schematics.

BBS
The software listings in this article are available on EDN's computer bulletin-board system (BBS). Phone (617) 558-4241 with modem settings 300/1200/2400 8,N,1. After signing on, enter "ss/freeware". Then enter "rkms839".

FPGA DESIGN-VERIFICATION ENVIRONMENT

You could use a gate-level simulator for design verification, but you generally do not have the option of coding an HDL design environment with a gate-level simulator. An HDL-based environment has a significant advantage over a gate-level environment. Gate-level simulators efficiently emulate networks of gates, but they can't run actual program code to generate complex signal-transition sequences. Typically, you must enter long sequences of test vectors to exercise a design. If a gate-level simulator offers any programmatic facility to aid in generating vectors, the programmatic facility is usually very limited. The HDL-based environment permits you to avoid the tedious job of generating vectors.

Design preparation

To make your design simulatable under an HDL simulator, you must first convert your design from the FPGA vendor's netlist format into the HDL. HDLs can simulate designs only in a certain format. After back-annotation, your FPGA design may be in the form of a netlist file, such as EDIF (Electronic Design Interchange Format) or a vendor-specific format. Luckily, these formats translate simply and directly into *structural* HDL.

Structural HDL specifies logic at the lowest level and, in many cases, invokes the raw FPGA macros. Structural HDL is the equivalent of a schematic in text form, whereas behavioral HDL specifies a design's operation by a computer-program segment. These behavioral program segments are usually more versatile, understandable, and maintainable than structural code.

Now that you have back-annotated your FPGA's netlist with timing information, you are ready to convert the netlist into the HDL's format. You perform this conversion using standard text-formatting utilities such as the Unix stream editors *awk* and *sed* (Ref 1) and GNU's more capable *perl* (Ref 2) along with an ASCII file-sorting utility. Learning how to program these utilites should take you no more than a day or two. If you work on a PC, you might want to exploit a word processor that offers a powerful macro language for this ASCII file conversion. But, I have never seen a text editor that

LISTING 1—COMBINATORIAL MODEL AND MAPPING EXAMPLE

```
library ieee;
use ieee.std_logic_1164.all;

entity aoi is
  port (signal a, b, c : in std_logic; signal y : out std_logic);
end aoi;

architecture structural of aoi is begin
  y <= (to_x01(a) and to_x01(b)) or to_x01(c);
end structural;

(a)
MM4983 : aoi
  port map(
    A => DS_8273'DELAYED(12.4 ns),
    B => OCTL_0_CCLRPEND'DELAYED(9.1 ns),
    C => OMS_BPWRITE'DELAYED(11.4 ns),
    Y => OCTL_0_116
  );
(b)
```

exhibits the flexibility and utility of *perl*. (PC versions of these programs are available.) This conversion job is straightforward because of the strict one-to-one mapping from gates and associated delays in the FPGA vendor's netlist format to gates and delays in the HDL.

Keeping this part of the method automated is important. If you do not let your computer do the work of reformatting netlists and other EDA tools' outputs, each recompilation of your design will require you to manually convert the FPGA's netlist into an HDL bus using a text editor.

You must also obtain a library for the gates your design uses. Some FPGA vendors may sell libraries for timing simulation of their parts in HDL source form. If not, writing models for a simulation library is not difficult. Combinatorial gates typically use a simple, per-input propagation-delay model. In such models, each input to the gate has a delay associated with it. The specified delay is the sum of the wire delay from the output driving the input and the delay from the input to the modeled gate output. Specifying such gates parametrically is trivial in an HDL gate model. Latches and flip-flops are more complex because of their requirement for checking input timing such as setup and hold times. But, you can also write latch and flip-flop modes with relative ease.

Fig 2a shows one FPGA design well-suited to verification

DESIGN VERIFICATION IS NOT THE SAME AS TESTING

Do not confuse this article's design verification with the action of a thorough set of test vectors. Test vectors toggle and observe all nodes in a chip to ensure that the chip itself is intact, but test vectors do not pay particular attention to the actual function of your design. Design verification, on the other hand, simply attempts to ensure that your design is correct for the application. Design verification ignores such testing obstacles as duplicated structures that operate correctly even if only one instance of the structure is correct.

For example, a set of thorough test vectors would pass ones and zeros

through each section of a 16-bit, 2-to-1 multiplexer. But, a design verification examines only a convenient subset of the multiplexer's functions, relying upon synthesis tools or macro definitions to ensure that untested portions of the multiplexer are correct. If a certain hexadecimal number goes into an input of the multiplexer and appears at the output, one side of the multiplexer's design is verified.

Test vectors are necessary for masked gate arrays to eliminate the cost of packaging chips that may be identified as nonfunctional at the wafer-probe stage. But, FPGAs do not necessarily need such

a set of test vectors. RAM-based FPGAs are completely tested at the factory and don't need additional testing. Makers test hard-wired FPGAs at their factories, and this testing provides a higher confidence level than with masked gate arrays.

Even in the case of hard-wired FPGAs, test vectors are not a necessity for every design, as long as in-system diagnostics and operational testing exercise the parts thoroughly. And, given the cost per gate of FPGA logic, inclusion of scan-path logic for testability is an option that many designers are not willing to consider.

using this article's techniques. The design is a display-list-based video-monitor controller. The FPGA formats display-list data from list memory and transfers the information to the serializer. The serializer then sends the data to the video monitor. The FPGA also arbitrates the microprocessor's access to the list memory.

To adapt this design to a design-verification environment, you must convert the netlist for the FPGA into the HDL and write models to emulate each of the system elements surrounding the FPGA.

For the most part, these surrounding models are probably behavioral models. Behavioral models respond to input-signal transitions by executing a computer-program fragment each time an input of interest changes. These program fragments can do just about anything a normal application program can: read and write files, maintain internal data structures, and print messages.

If you carefully apply this sequential, programlike behavior, you can expeditiously emulate behavior that would be too complex to implement with a structural model. This programlike behavior can also provide high-level indications of a design's functions that a human can easily understand and examine. Probably, the most valuable aspect of using behavioral models for design verification is that you do not have to verify a circuit's functions via tedious and error-prone examination of ones and zeros. Instead, the model formats the information into its most recognizable form for quick, high-confidence examination.

Fig 2b shows the modeled equivalent of the system. The microprocessor model performs reads and writes specified in an access file. The list memory reads in its contents upon initialization but otherwise behaves like a static RAM.

The video-monitor model performs serial-to-parallel conversions of data from the serializer and outputs the information to a sequence of raster files. You can physically output the raster files later to a graphics screen and verify the

LISTING 2—FLIP-FLOP MODEL AND MAPPING EXAMPLE

```

library ieee;
use ieee.std_logic_1164.all;

entity dfc1 is
  generic (
    constant tHASYNC, tHD, tPWASYNC, tPWCLK, tRECASYNC, tSUD
    : in time := 0 ns
  );
  port (
    signal clk, clr, d : in std_logic;
    signal q : inout std_logic := 'W'
  );
end dfc1;

architecture sequential of dfc1 is
begin
  process (d,clk,clr,q)
    variable firsttime : boolean := true;
  begin
    if (firsttime and q'EVENT and (q = '0' or q = '1')) then
      q <= q;                                         -- latch forced state
      firsttime := false;
    end if;
    if (clr = '0') then
      if (clk'EVENT and clk = '1') then
        assert now-d'LAST_EVENT > tSUD
        report ("DFP d setup violation")
        severity ERROR;
        if (to_x01(d) = 'X') then -- prevent unknown flood
          q <= '0';
        else
          q <= to_x01(d);
        end if;
        firsttime := false;
      end if;
      assert not (d'EVENT and clk'LAST_EVENT < tHD)
      report ("DFP d hold violation")
      severity ERROR;
    end if;
    if (clr = '1') then
      q <= '0';
    end if;
  end process;
end sequential;

```

(a)

```

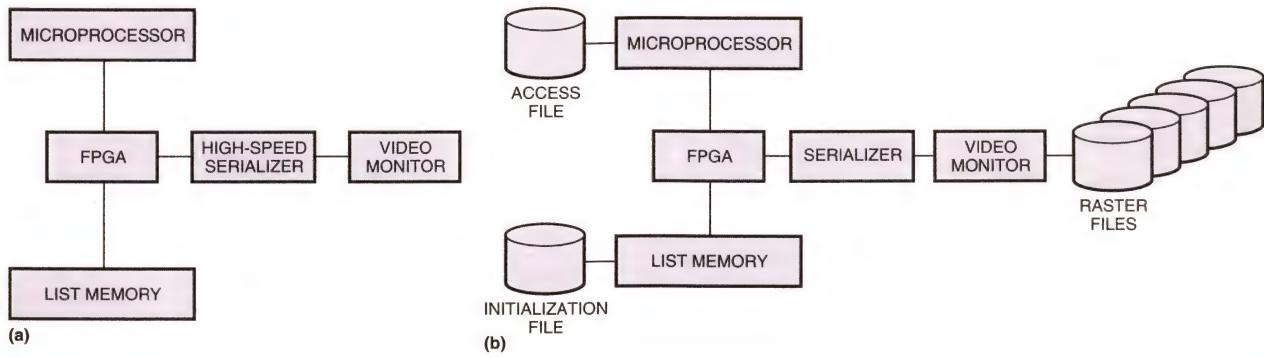
MM4984 : dfc1
  generic map(
    tHD => 0 ns,
    tPWCLK => 7.9 ns,
    tSUD => 0.7 ns
  )
  port map(
    CLK => CLOCKT'DELAYED(14.5 ns),
    D => OCTL_0_SPCHTXC_D'DELAYED(7.7 ns),
    Q => SPCHTXC
  );

```

(b)

raster files visually. Viewing the raster files is a powerful verification tool that provides a level of confidence that you could never achieve by simply examining signal traces in the simulator. For instance, if an arbiter bug in the FPGA were

FIGURE 2



The design in (a) is a display-list-based video-monitor controller. Its FPGA formats display-list data from list memory and transfers it to the serializer, which sends the data to the video monitor. The FPGA also arbitrates the microprocessor's access to the list memory; (b) is the modeled equivalent of the system in (a). The microprocessor model performs reads and writes specified in an access file.

FPGA DESIGN-VERIFICATION ENVIRONMENT

causing the microprocessor's accesses to corrupt the output to the monitor, the problem would be immediately apparent in the raster output.

High-level verification of this sort is not limited to this design. The general principle applies to many types of designs. A word of caution: This technique is not a substitute for a conscientious examination of the entire simulation output. Each design has its own set of subtle failure modes and bugs that requires your close attention. High-level verification remains a crucial tool, but not the total solution.

Model implementation

The remaining portion of this article details actual HDL examples of typical models. The code is in VHDL (Refs 3 and 4), although the general principles should apply other HDLs as well. The VHDL *value system* used is the IEEE standard *std_logic_1164* package. The term "value system" refers to a set of possible logic values that a signal may carry: "X" for unknown, "1," "0," and many others. The VHDL references clarify the exact use of these values.

Perhaps the simplest HDL models to write are models for combinatorial gates in your FPGA's library. In Listing 1a,

the model for an AND/OR gate uses a simple, concurrent signal assignment to model the gate. The *architecture* section specifies the logical relationship between the inputs *a*, *b*, *c*, and the output *y*. The function *to_x01()* converts the nine-valued *std_logic* signals into the simple "x," "0," and "1" values suitable for use by the signal assignment.

Listing 1b shows an actual invocation of Listing 1a's gate in the converted FPGA netlist. The numbers in the *DELAYED* clauses come directly from the back-annotated wire delays. The *port map* statement associates each of the pins of the model (*a*, *b*, *c*, and *y*) with an actual signal. For each of the inputs, the *port map* statement also specifies the delay from the driving pin on the signal to the associated input. The term for these delays is "wire delays." The back-annotation program inserts these wire delays into FPGA netlists. In front of the invocation, *MM4983* is a slightly modified form of the label for the gate as it appeared in the original FPGA netlist.

Flip-flop model

The FPGA-simulation library (and possibly the models in the environment) may need another model, such as a flip-flop or latch. Listing 2a shows a basic flip-flop model from

LISTING 3—MICROPROCESSOR MODEL

```

library ieee;
use ieee.std_logic_1164.all;
use std.textio.all;
use work.io_utils.all;

entity mp is
  port (
    clock : in std_logic;           -- clock for
    delays
    md : inout std_logic_vector(7 downto 0); -- uP data
    ma : inout std_logic_vector(14 downto 0); -- uP address
    csN : inout std_logic := '1';          -- slave chip
    select
    wrN : inout std_logic := '1';          -- uP write
    strobe
    rdN : inout std_logic := '1';          -- uP output
    strobe
    ack : in std_logic;                  -- acknowledge
    pulse
    );
  end;

  architecture sequential of mp is
    -- Timings
    constant tARSU : time := 40 ns;      -- address
    constant tSTB : time := 45 ns;        -- strobe deassertion
    delay
    constant tRDSU : time := 20 ns;       -- read data setup to
    ack
    constant tBTO : time := 10 us;        -- bus timeout
    constant tTOCL : time := 600 ns;       -- bus timeout clear
    time

    procedure ackwait is begin
      wait on ack for tBTO;
      if not rising_edge(ack) then
        assert false
          report "uP timeout waiting for ack"
          severity error;
      end if;
      end ackwait;

    begin
      process
        file f : text is in "mp.dat";      -- bus cycler
        variable l : line;                -- input record
        variable l1 : line;                -- output print
      record
        variable ok : integer := 0;        -- clock specifier
        variable addr, data : integer;     -- numeric command
      fields
        variable rw : character;          -- read/write select
        variable currentclock : integer := 0; -- clock cycle
      counter
        variable tmp : std_logic_vector(31 downto 0); -- VHDL
      begin
        readline(f,l);
        while not(endfile(f)) loop
          while l'LENGTH /= 0 and l(1) = '#' loop -- skip
            readline(f,l);
          end loop;
          if l'LENGTH /= 0 then
            -- skip blank
          end if;
        end loop;
      end process;
    lines
  end;

```

```

    -- Get fields
    -- Format: <clock number> r|w <address> [<data>]
    read(l,ck);
    read(l,rv);
    read(l,addr,16);
    if rw = 'w' then
      read(l,data,16);
    end if;
    -- Wait for the specified clock cycle
    while (currentclock < ck) loop
      wait on clock;
      if (clock = '1') then
        currentclock := currentclock+1;
      end if;
    end loop;
    -- Execute the bus cycle
    tmp := to_x01(addr);           -- drive address
    ma <= tmp(14 downto 0);         -- chip select
    csN <= '0';                   -- read cycle
    if rw = 'r' then
      md <= "ZZZZZZZZ";
      wait for tARSU;
      rdN <= '0';
      ackwait;
      if not rising_edge(ack) then -- timeout
        rdN <= '1';
        csN <= '1';
        wait for tTOCL;
      end if;
      assert md'LAST_EVENT >= tRDSU
        report "MP data to ack setup
      severity error;
      data := to_int(md);           -- print read data
      write(l1, string'("Memory read "));
      write(l1,addr,right,4,hex, false);
      write(l1,string'(" returns "));
      write(l1,data,right,2,hex, false);
      writeln(output,l1);
    elsif rw = 'w' then           -- write cycle
      tmp := to_x01(data);
      md <= tmp(7 downto 0);
      wait for tARSU;
      wrN <= '0';
      ackwait;
      if not rising_edge(ack) then -- timeout
        wrN <= '1';
        csN <= '1';
        wait for tTOCL;
      end if;
      wait for tSTB;
      wrN <= '1';
      rdN <= '1';
      csN <= '1';
      wait on ack;                -- deassertion
      end if;
      readline(f,l);
    end loop;
    wait until false;             -- next record
  end process;
  end sequential;

```

SEMICONDUCTORS

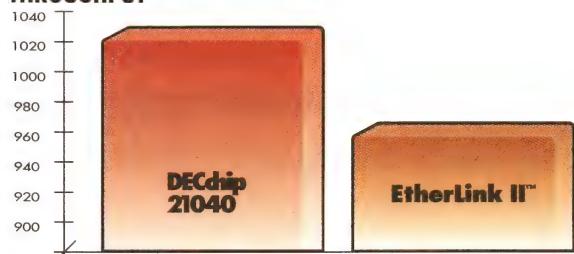
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which you can build other variants. You can model variants with differences, such as complemented clock inputs or missing clear signals, simply by including the basic model inside the variant model and complementing the clock input or tying the basic model's clear signal inactive.

You must determine exactly how many timing-parameter checks make sense for your application. For example, many single-clock synchronous designs have a synchronized global reset connected to their flip-flops' asynchronous-reset inputs. These designs use this reset line only once upon power-up. In these cases, the flip-flop model needs to check only the setup time between data and clock. The model can probably safely ignore parameters such as clock pulse width and reset recovery time. This limited checking can simplify the model. The model in **Listing 2a** checks only setup and hold times. If a setup or hold time is violated, the model prints a violation message to the simulator's screen.

Another important issue is reset behavior. Some FPGAs require that you explicitly route an asynchronous reset signal to each flip-flop that needs to be reset. For those devices, you can save resources by resetting only flip-flops that need resetting and permitting other flip-flops to decay to a quiescent state after some number of clock cycles has elapsed.

In designs of this type, the time required to reach the quiescent state may be too long to simulate. You need some mechanism that allows the simulation to leave the reset critical flip-flops in an initial unknown state at the beginning of the simulation and initializes the noncritical flip-flops to avoid having to wait for them to settle to their quiescent state.

The model in **Listing 2a** declares its *q* output as an *inout*, meaning that changes of state due to external forcing of the output by the simulator are visible to the model. The initial state of the *q* output is "W", or a weak unknown, that will drive an unknown state if such driving is important to the simulation. If such driving is not important, you force the flip-flop's *q* output to the desired state at the beginning of the simulation script, and the *if* statement at the beginning of

the model detects the force and accepts whatever state you have forced for the driven *q* state.

The model also propagates a zero if an "X" or unknown is clocked into it. This action prevents an unknown flip-flop state from propagating to other flip-flops in your design and then consuming an inordinate number of clock cycles for the unknown states to decay away. Such behavior provides little value in design verification, and this tradeoff can save much simulation time with little loss of fault coverage.

Listing 2b shows an invocation of the flip-flop, using the

LISTING 4—SELF-SCHEDULING RAM MODEL

```

entity ram is
  port (
    d : inout std_logic_vector(15 downto 0); -- data
    a : in std_logic_vector(14 downto 0); -- address
    ceN : in std_logic; -- chip enable
    ...
  );
end;

architecture sequential of ram is
  signal s : boolean; -- self schedule
  request
    type memory is array (0 to 32768) of integer;
    variable ramdat memory;
  ...
  process (a,d,ceN,...,s' TRANSACTION) -- sensitivity list
    variable ce : std_logic; -- ce logical value
    variable tmp : std_logic_vector(31 downto 0); -- VHDL
    begin
      if a'EVENT then -- address line
        changes
          s <= '1' after tACC;
        end if;
      if ceN'EVENT then -- chip select
        changes
          s <= '1' after tCO;
        end if;
      ...
      ce := not to_x01(ceN);
      -- valid read access
      if not a'EVENT and now-a'LAST_EVENT >= tACC and
         not ceN'EVENT and now-ce'LAST_EVENT >= tCO and ce = '1'
      then
        if not is_x(a) then
          tmp := to_x01(ramdat(to_int(a)));
          d <= tmp(15 downto 0);
        else
          d <= "XXXXXXXXXXXXXXXXXXXX";
        end if;
      end if;
    end process;
  end sequential;
end;

```

THE SIMULATION-VS-PROTOTYPING TRADEOFF

The first revision of an FPGA usually still has bugs in it, even after simulation. Ten seconds of real time in a functional system can easily be worth days of simulation time. Bugs that show up only in the real world don't mean that design verification is pointless, though. Simulating a design up to some judiciously chosen point can uncover bugs that would take longer to find in an actual prototype.

You must base your choice of much verification to do with a simulator and how much to leave to actual hardware debugging on an analysis of the cost in verification time vs the benefit in debugging time. Design verification should

attempt to probe those areas in your design where the greatest questions about your design's integrity exist.

For example, interfaces between microprocessors and static memory are straightforward. Compared to large blocks of custom control having complex state sequences, memory interfaces need little attention.

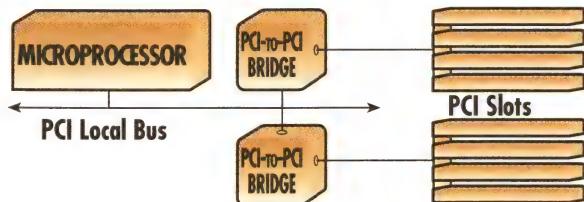
The law of diminishing returns applies to design verification. If a simulation makes your design's most basic and frequent operations visible, you can consider your design to be 50% covered. If the simulation exercises all state sequences, then a typical design is prob-

ably more than 90% covered. But, as coverage increases, each successive increment requires more effort and simulation time. Soon, you reach the point where leaving the last amount of coverage to actual operational test and diagnostic software is more economical.

A simple plan would be to first write simulations that exercise all state sequences. Then, spend some time developing simulations that generate asynchronous stimuli for your design. The exact tradeoff between preprototype and postprototype verifying depends very much on your design and judgment.

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VHDL DELAYED construct for signal-wire delays. The VHDL GENERIC clause passes back-annotated timing parameters for the flip-flop into the model.

Proving that this flip-flop model does not behave exactly like an actual circuit is easy. The model trades robust behavior for shorter development time. Although less robust, the model remains quite usable for design verification. A useful model does not need to be precise in every detail. You can save a significant amount of time if you identify just how complex a model's behavior must be for your application and then implement only to that level.

Microprocessor model

Frequently, design verification requires a microprocessor model that exercises a slave device and accesses the device using varying timing, addresses, and data patterns. Listing 3 shows a model for a microprocessor that reads access commands sequentially from a command file, *mp.dat*. Each command line of the command file contains a read or write indicator, an address, and optional data. For legibility and documentation's sake, the model permits blank lines and comments beginning with "#." The results of each read also get printed to the simulation console.

At the top of Listing 3 are specifications for all of the timings for the model in symbolic form. You could code these times directly into the listing where they are used, but the result is not as readable, and changes to the timings are more difficult to make. In general, using this kind of symbolic abstraction to improve the readability and maintainability of a model is a good idea.

At the beginning of each command line that the model reads from the command file is a clock-cycle number. The

model uses these numbers to time accesses. The model counts clock cycles and, when the requested clock cycle occurs, performs the specified access. Accesses wait for an acknowledge on the *ack* signal, timing out if no response occurs.

This microprocessor model demonstrates the power of behavioral models for design verification. A sequential program simulates the behavior of the microprocessor. Writing a state-machine implementation of the microprocessor model is much more difficult to do than writing the behavioral model in Listing 3.

RAM models

Often, simulations need RAM. The complex timing behavior of RAMs makes a robust RAM model a valuable tool in timing simulation. Proper RAM operation involves meeting numerous setup-and-hold specifications that make a typical RAM model fairly large. A usable static-RAM model that performs timing-violation checks can be 300 lines or more in length.

Although reproducing a RAM model in its entirety is beyond the scope of this article, there are some important points about RAM-model coding to consider. First, you can save simulation time if the model initializes itself from a data file upon simulation start-up and uses file I/O similar to the microprocessor model's.

Second, simulators usually incorporate a sensitivity-list mechanism that tells the simulator explicitly which signals cause execution of a model when they change. In the case of the AND/OR gate in Listing 1a, the model executes each time one of its inputs, *a*, *b*, or *c*, changes.

Using specialized model scheduling can produce a mini-

COMMERCIAL MODELS EXHIBIT GOOD POINTS, BAD POINTS

For a price, third-party models are available for microprocessors, memories, and other functions. You could incorporate them in your design-verification environment. When considering commercial models, you should review the following factors:

- Because of the vendor's time dedicated to developing these models, you can reasonably assume that they are more robust than a simulation model that you have written. If the model is a complex one—for example, a bus-snooping microprocessor model—your effort to produce an accurate model from scratch may outweigh the cost of the model. Such a model may require a design verification before you can use it. Models that you code are not a capital investment. The only cost involved is design time, and for models of limited complexity, the

time investment is not large.

- Commercial models may not suit your task. The set of all possible models for all possible parts will never exist, so, if you use commercial models, you need to make compromises in your verification environment. These compromises may translate into inefficiency or ineffectiveness.
- A commercial model may be more than you need, given its cost.

For example, you might need a FIFO model that is only 13 bits deep, prints a message on overflow, and centers its write pointer when overflow occurs. A commercial model is probably unable to meet these exact requirements.

On the other hand, a commercial microprocessor model could accurately simulate instruction prefetch, caching, and other complex behavior. But you may need a model that drives

only the address and data lines, toggles a strobe, then waits for an acknowledge. In this case, given the simplicity of a model you could code, the cost of the more complex model may not be justified.

Model vendors must provide as many options as possible, but the question remains whether you can optimize a commercial model to meet all the requirements of an efficient simulation. If you have total control of the model's source code, no such question arises. You can adapt your own model in the finest detail to the needs of your design-verification environment.

You may also wish to simulate a simple piece of discrete glue logic without having to purchase an entire library of 7400-series TTL models. You could accomplish this task in very few lines of a modeling language at virtually no cost.

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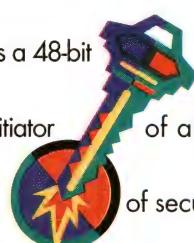
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mally complex, understandable model. Simulators usually incorporate a scheduling mechanism that models delay. For instance, if a model contains the statement

`a <= b AFTER 20 nsec;`

the simulator schedules a change on signal *a* 20 nsec after each change on signal *b*.

For a part with as many signal-to-signal timing constraints as a RAM, an effective way to test for timing violations is using self-scheduling. Self-scheduling uses the simulator's scheduling mechanism along with the sensitivity-list mechanism to permit the model to schedule a timing check after an input transition. Self-scheduling causes a model to reschedule its own execution after the transition of a signal of interest.

To perform self-scheduling, the model declares a dummy input/output signal in its sensitivity list only for scheduling purposes. When the model must schedule an execution, it simply makes an assignment to that signal using either an AFTER clause or its equivalent. Because the signal is on the sensitivity list, the model re-executes after the specified time.

Self-scheduling is particularly useful when a model's input signals must satisfy multiple time constraints before an output signal becomes valid. RAM read accesses are such a case. Consider a RAM with an output that is valid subject to address access time, *tACC*, and chip-enable access time, *tCO*. Listing 4 shows portions of a RAM model that validate both of these times using self-scheduling. For simplicity's sake, the example disregards other signals and timing parameters for the RAM.

In the upper part of the *process* in Listing 4, changes on the address and chip-select lines cause the model to reschedule an evaluation after *tACC* or *tCO* has elapsed. At that time, the lower part of the model validates a read access by checking to see if the access times have met *tACC* and *tCO*.

The TRANSACTION attribute specified for the scheduling variable in the sensitivity list causes model evaluation whenever the simulation makes an assignment to the scheduling variable, whether or not the variable changes state. Unlike the mechanics of common programming languages in VHDL, making an assignment does not necessarily change the state of a VHDL variable. VHDL can recognize an assignment even if the assignment has no physical counterpart in a real system. A variable with a "1" state, however, retains that state if it's assigned the value "1."

Note: The model may require some modification and work to get it to function as intended. For example, some VHDL simulators do not handle the LAST_EVENT attribute in the way that you might expect. In the actual RAM model (see Listing 4), I had to emulate the LAST_EVENT attribute in VHDL to produce the desired function.

Also, in the simulator I used, the TRANSACTION attribute did not always schedule re-evaluations as it should have. To work around this problem, I declared the scheduling variable as an array of type *boolean* and sequentially made rescheduling assignments to each of the elements in the array in a rotating fashion. Simulators are not without bugs.

RAM models are the most difficult of the models discussed in this article to write. If robustness of the RAM model is critical, you may need to build a small simulation to verify the RAM model before using it in design verification. If you are

LISTING 5—TEST-CASE-DEPENDENT OSCILLATOR MODEL

```
library ieee;
use ieee.std_logic_1164.all;

entity osc is
  port (
    testno : in integer;           -- test number controls
    behavior
    clock : inout std_logic := '0'
  );
end;

architecture sequential of osc is
  constant tCLK : time := 100 ns;           -- normal clock
  period
  begin
    process (clock)
      variable tCLKx : time;           -- calculated clock period
      begin
        if testno = 2 or testno = 6 or testno = 11 then
          tCLKx := tCLK/2;
        else
          tCLKx := tCLK;
        end if;
        clock <= not clock after tCLKx/2;
      end process;
    end sequential;
```

not relying on the model for timing verification, seeing the model work properly in your design-verification environment can be sufficient proof of its integrity. I use the second approach in conjunction with a static-timing analysis to yield a functional product with no known RAM-timing problems.

Static-timing analysis

In general, timing simulation does not guarantee that a design meets timing requirements. Producing a simulation that exercises all the paths in a design can be a challenging task, especially if a synthesis tool produces the gate-level netlist. If you have produced models with timing checks in them, at least some of the checks will contain bugs that permit timing violations to go unnoticed.

In the type of design-verification environment described here, you should use timing simulation only as a reinforcement to timing verification using a static-timing-analysis tool. Static-timing analysis exposes all paths in a design, regardless of logic structure. A static analysis with an output that is used in a conscientiously prepared, hand-done, or spreadsheet-based, system-level timing analysis should expose any timing-check inadequacies in your design-verification models. Even if your models have no bugs, the thoroughness of a static analysis provides much more confidence in your design's timing than does timing simulation.

Design-verification techniques

Some general techniques that can make your design-verification environment more robust and efficient include global test numbering and software testing during simulation.

At the highest level, you should automate your test environment to make the most efficient use of your time. For example, suppose a model needs to change its function from test case to test case. You should consider writing the model to modify its function based on a test number connected to an input on each of the models in the simulation environment.

A simple example of this technique would be an oscillator that runs at twice the normal speed for certain test cases. Listing 5 shows a model for an oscillator that does this for test numbers 2, 6, and 11.

The top-level netlist connects the *testno* inputs of all sim-

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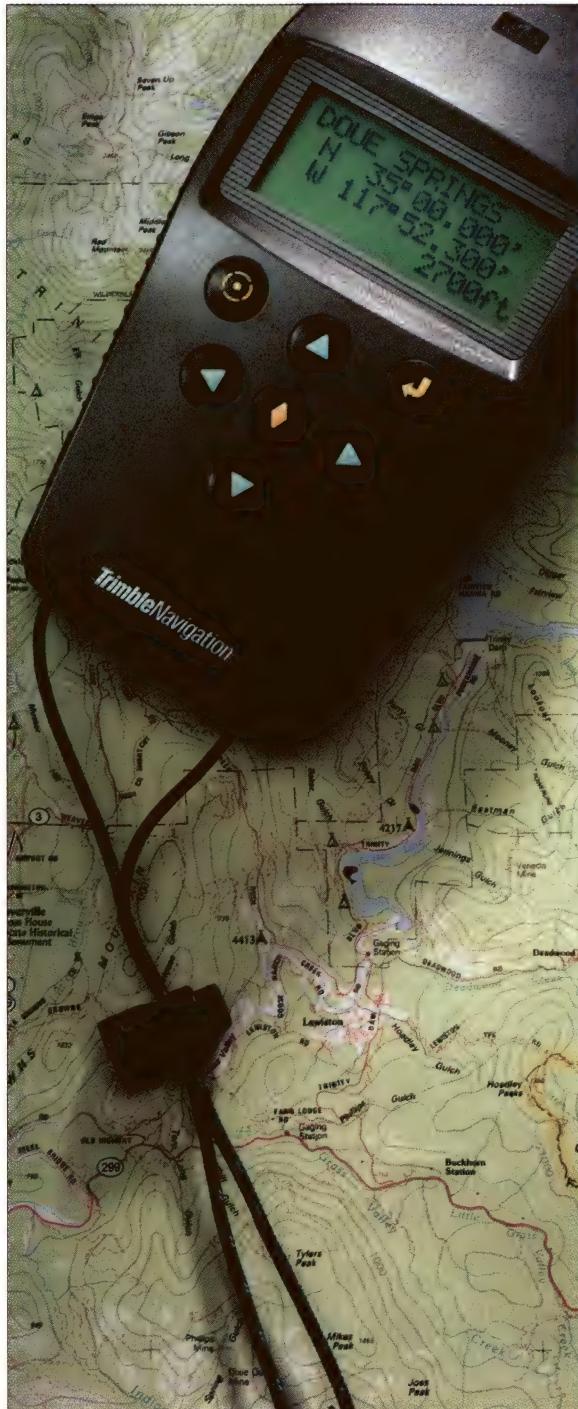
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ulation models that are connected. The simulation script sets *testno* equal to the test number at the beginning of the script. This technique is preferable to editing and recompiling the model to change its behavior.

You can design your environment to use test-execution scripts at the highest level. These scripts select an entire set of simulation inputs, such as microprocessor access files and RAM data files, based on a single test number that is part of the test script's invocation. This technique provides you with more time to concentrate on the actual debugging of your design instead of the mechanics of simulation.

Another technique worth consideration involves joint testing of driver software and hardware. The driver software that manages the details of a design's operation often consists of a set of access routines and bit-field definition symbols, all of which you must debug. Rather than input all stimuli (RAM contents, etc) to your design in binary, you should construct the driver software so that parts of it may function as an application program if the appropriate compile switches are set.

This application program may then generate input data files for simulation using exactly the same symbolic constructs that the device-driver programmer uses. This approach has two advantages: You save the time and trouble of generating potentially lengthy sets of binary data to exercise your design, and the programmer is confident that his symbolic representation of your design is correct. Using symbolic representations instead of machine-based representations results in a net time savings.

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Leo Bredehoft is an engineer for Netrix Telecom Systems in Boulder, CO, and he has worked there for 3½ years. He specializes in digital and FPGA design, software, and diagnostic-software design. He has worked on telecommunications equipment, such as cross-connect and a time-division multiplexer. He obtained a BSEE from Wichita State University, Wichita, KS, and he is a member of Eta Kappa Nu, Tau Beta Pi, and Phi Kappa Phi. In his spare time, he enjoys playing classical piano and studying foreign languages.

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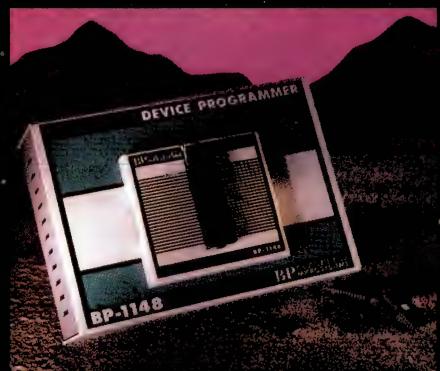
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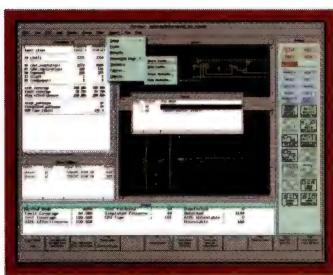
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Green strategies cope with electronic products' energy and end of life

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Engineers must be aware of the alternatives that make a system "green," but what are the guidelines for choosing the best options? Although design-for-environment (DFE) tools are available, they are at best crude. Engineers are "hampered by lack of comparative-risk information; lack of a method of comparing unlike risks; and a lack of a method for integrating risk, performance, and cost information into a decision-focused system," stated Jean Parker of the Environmental Protection Agency's Design for the Environment Program during the 1993 Electronics and Environment Symposium. Nonetheless, techniques are emerging to help make the right choices. Those techniques include life-cycle analysis (LCA), energy audits, pollution-prevention checklists, and guidelines for parts/material recovery and recycling.

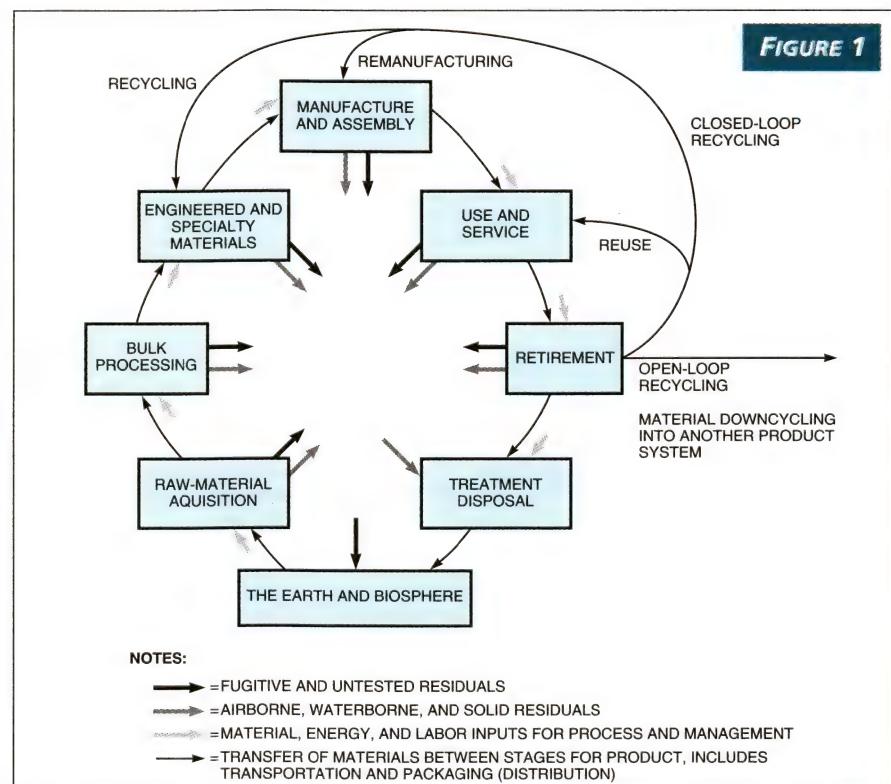
LCA is a good starting point. The term refers to the overall process by which one evaluates all environmental impacts from acquiring raw materials, through manufacturing and use, to the final disposing of a product. In laying out the conceptual framework for LCA, James A Fava, a pioneer in the field, points out that the outlook in the '90s has moved beyond that of the '70s and '80s. The focus was once on constraining the discharge of pollutants into the air, water, and land. But in the 1990s, the EPA switched from pollution control to pollution prevention. The objective is to cut pollution to zero using natural ecosystems as the model. Industrial systems should not be open-ended, dumping endless byproducts, but closed, as nature is, cycling and recycling.

The practice of LCA stems largely

Emerging design-for-environment techniques will help keep Mother Earth green.

from a basic text published by the Society of Environment Toxicology and Chemistry (SETAC) (Ref 1). *Technical Framework for Life-Cycle Assessment* states that companies can best begin LCA with senior management's commitment to improve the environmental quality of the company's products or manufacturing. This usually entails identifying the key functions associated with a product from R&D through marketing and sales to customer use and disposal. A team approach is necessary. Fava advises asking such questions as:

- What is the source of the raw materials?



The product life-cycle system is a closed loop that involves the earth and biosphere. Reuse, remanufacturing, and recycling can create other loops that counterbalance the system. (Source: EPA's *Life Cycle Design Guidance Manual*).

DESIGN-FOR-ENVIRONMENT TOOLS

- Is the product highly dependent on nonrenewable resources?
- How much energy does the product use?
- Does the product's manufacture require highly energy-intensive processes?
- Does the product or process require extensive use of water?
- Are transportation costs high?
- Does manufacture or transportation cause excessive release of carbon dioxide?
- Can the product be easily recovered and recycled or reused?

A reference manual shows the way

The publication in Ref 2 provides another basic LCA tool. Fig 1 portrays that book's product life-cycle system, and Fig 2 provides a schematic of life-cycle design. Fig 3 depicts matrices to conceptualize environmental requirements and performance. In developing environmental requirements, first take stock of the materials used. Table 1 lists factors you should consider, and Table 2 lists how AT&T applies these principles in a demonstration project with the University of Michigan.

In its simplest form, LCA comprises three stages: taking inventory, assessing impact, and assessing improvements (Fig 4). Taking inventory, the most developed component of

ENERGY STAR SAVINGS MOUNT

The Environmental Protection Agency (EPA) predicts that the demand for electrical energy will rise 1 to 1.5% per year through 2000. However, Dennis McGavin of Hewlett-Packard believes that residential energy demand could be 25% less if consumers bought energy-efficient appliances. Commercial and residential energy use is decreasing as manufacturers join the EPA's Energy Star, a voluntary program to induce manufacturers to produce more energy-efficient products. Energy Star logos appear on products consuming no more than 30W.

EPA estimates that manufacturers of laser printers, for example, could cut energy consumption 30 to 50%. The reduced consumption would save 6 billion kWh in 2000, thereby reducing electricity bills by \$500 million and avoiding annual carbon emission equal to that produced by 1 million cars. HP, a member of the Energy Star program, has four printer lines and the Vectra PC (including monitor) that qualify for a logo.

LCA, involves using a database that quantifies energy and raw-material requirements (inputs) and environmental outputs, such as air emissions, water effluents, and solid and hazardous waste for the life cycle of the product. Energy inputs can take into account transformation cost (raw materials into products), transportation cost (running assembly-line conveyors), and any reduction cost (when using recycled materials). Michigan State University has developed mathematical system models quantifying such inputs for given boundary limits.

Impact assessment is harder to perform. Certain materials, processes, or components may be toxic, but their impact on the environment and health varies, according to the amounts involved. For example, when evaluating a given design, you may have to decide what weights to give carbon-dioxide release compared with sulfur dioxide. If you use disposable or rechargeable batteries, how do you weigh performance (battery-charge life) against toxicity? You have to make and record value judgments so that others understand the basis for your rating.

Some companies are working to incorporate life-cycle costs and life-cycle cost-management calculations into LCA. One such company, Decision Focus Inc, Mountain View, CA, uses the Generalized Equilibrium Modeling System and proprietary CAD/CAE software. Another company doing economic modeling in DFE is Synergy International, Atlanta. Synergy provides "activity models" and reports that the US Air Force developed IDEF, a comput-

TABLE 1—ISSUES FOR DEVELOPING ENVIRONMENTAL REQUIREMENTS

		Materials		Impacts associated with extraction, processing, and use
Amount (intensiveness)	Type	Character		
	Direct	Virgin		Residuals
	Product related	Recovered (recycled)		Energy
	Process related	Reusable/recyclable		Ecological factors
	Indirect	Useful life		Health and safety
	Fixed capital (Building and equipment)	Resource base factors		
		Location		
		Locally available		
		Regionally available		
		Scarcity		
	Source	Threatened species		
	Renewable	Reserve base		
	Forestry	Quality		
	Fishery	Composition		
	Agriculture	Concentration		
	Nonrenewable	Management/restoration practices		
	Metals			
	Nonmetals	Sustainability		
		Energy		
Amount (energy efficiency)	Type	Character		Impacts associated with extraction, processing, and use
	Purchased	Resource base factors		Materials
	Process byproduct	Location		Residuals
	Embodied in materials	Scarcity		Ecological factors
	Source	Quality		Health and safety
	Renewable	Management/ restoration practices		Net energy
	Wind			
	Solar			
	Hydro			
	Geothermal			
	Biomass			
	Nonrenewable			
	Fossil fuel			
	Nuclear			

(Source: EPA's *Life Cycle Design Guidance Manual*)

er-aided software-engineering tool, for defining complex sets of interacting activities in the life cycle of an aircraft.

LCA impacts electronics

Although LCA emerged to analyze manufacturing, particularly those involving toxic chemicals, it will soon affect all electronic sectors. The energy-efficient "green PC" is one example. Computers account for about 5% of all commercial energy in use today, and this may double by 2000, says Jacques Besnainou of Ecobalance (Wayne, NJ). "LCAs that encompass the entire life cycle of a product from raw-material extraction to end-of-life management alternatives (landfilling, incineration, and recycling) provide an unbiased map of industry systems." Besnainou says the reusable-vs-recycling and recycling-vs-incineration debates are complex and not as green as you might assume. For example, nickel alloy contacts in switches are not better than the more toxic alloys when you consider the total life of the switch.

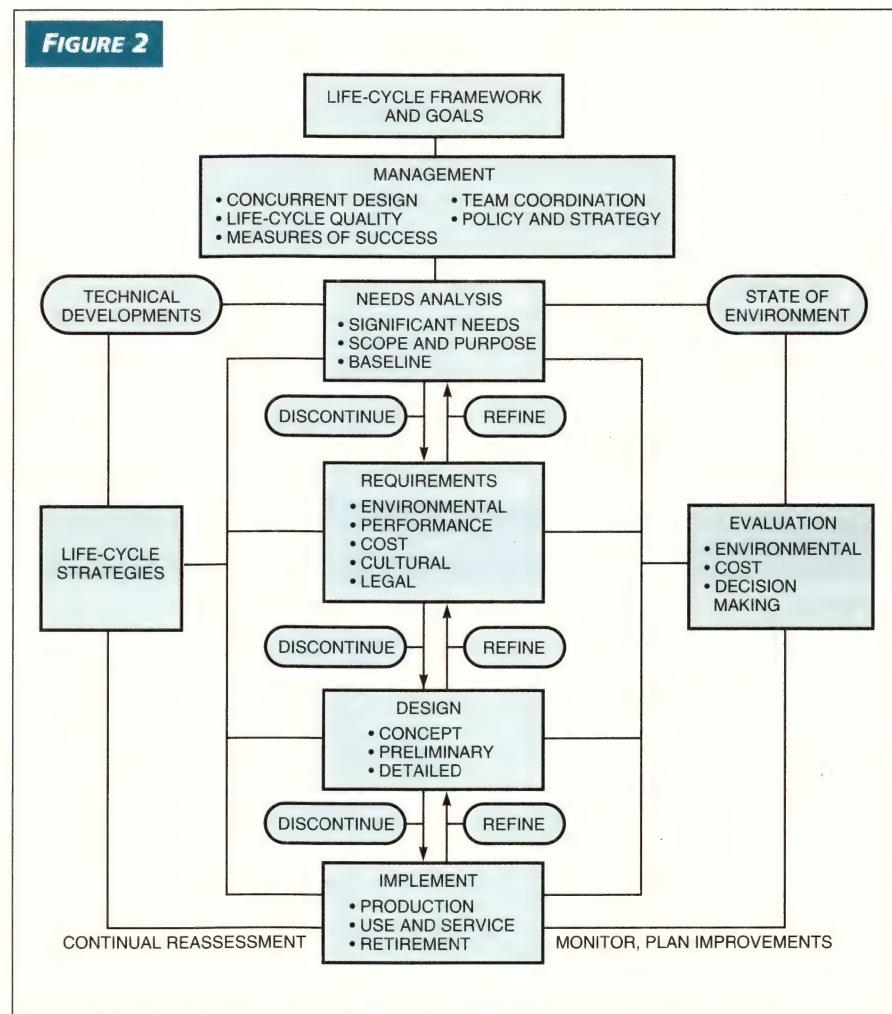
The Life Cycle Center of the Technical University of Denmark, Lyngby, Denmark has made a detailed analysis of energy consumption for a frequency converter and a portable telephone. As Jens Legarth, an engineer at the Institute for Product Development at the University, told the 1994 Electronics & Environment Symposium, "Great rewards result from reducing energy consumption in *all* life-cycle phases."

The Life Cycle Center maps and quantifies all environmental impacts from all life-cycle phases—raw-material extraction, production use, transportation, and customer use. Customer use of a product is the major contributor to smog, nitrogen oxides, acid rain, and carbon-dioxide release—all stemming from a product's energy consumption. Higher efficiency converters can reduce the impact.

The Life Cycle Center normalizes all data by dividing it by a reference emission, based on the equivalent per-year per-world citizen. The Center expresses a product's contribution to global warming as a person equivalent. In the study of the portable phone, energy spent in production turned out to be greater than lifetime use, but the energy expended in production included that for not only material transformation but also the energy channeled to keep factory and headquarters workers comfortable (such as heating and air conditioning).

Switching power supplies generally operate at 75 to 80% efficiency, according to Charles Sullivan, an engineer and member of the computer department of the University of California at Berkeley. He believes that 95% efficiency should not be difficult to achieve. In any case, switching power supplies are superior to linear units, which are approximately

FIGURE 2



Life-cycle design comprises a management strategy that oversees a continuously refined closed-loop system. (Source: EPA's *Life Cycle Design Guidance Manual*).

50% efficient and require expensive transformers and capacitors. He points out that you must consider the duty cycle of a product's power demands. Standby or idle power for a telephone-answering machine is greater than the power consumed during operation. In the design of portable computers, power management ranks in importance with computing capability.

Sullivan points out that you must consider full product life—not short-term—power costs because the least expensive component for a job may be the most costly in the long run. For a 2.5A circuit requirement, a \$3.30 MOSFET overrated at 18A operating over five years has a total cost of \$6.29 compared with \$25.58 for a \$0.98 MOSFET that handles 2.5A. In another example, Sullivan determines that a line-powered electronic clock costing \$10 consumes nearly that much cost in electricity in 10 years. LEDs use more power than LCDs, he adds. Sullivan also suggests that there is considerable room for reducing clock power because no electronic timekeeping device on the market uses less than 10 μ W.

If end-of-life products go into landfills, waste can never be reduced to zero. Western industrial countries are rapidly closing their landfills. US landfills will number 3250 by 2000, for example, compared with 18,500 in 1979. However, electrical

DESIGN-FOR-ENVIRONMENT TOOLS

and electronic products that need disposal are doubling. Germany is dumping 1 million to 1.5 million tons of used electronic products annually, with TV sets accounting for almost 60% by weight. A study in France, the Desgeorges Report, found that 1.3 million tons of electrical products are now reaching end of life. Nearly twice that amount is entering the market, so the problem of electrical waste is getting worse. Commercial/industrial electrical products account for 31% of electrical waste; appliances, for 29%; batteries, for 14%; consumer electronics and cable, for 8% each; computer office equipment, lighting fixtures/lamps, and "other," for 3% each; and telecommunications, for 1%. Computer waste is the growth factor. If things don't change, Americans could be dumping 150 million PCs by 2005, according to another study.

To cope with the waste problem, Europe has pending leg-

islation that calls for manufacturers to take back the products they produce. Both the Netherlands and Germany are close to passing such laws. Computer companies are looking at the "six Rs" of DFE: reduce, reuse, reclaim, refurbish, remanufacture, and recycle. Take-backs add to the costs of products, but some companies, such as Digital Equipment Corp, Hewlett-Packard, and Xerox, see a potential cost benefit from recycled materials according to Dave Williams, a professor at Loughborough University in the United Kingdom, who interviewed these and other manufacturers.

HP is recycling 65% of its hardware in Europe, Williams reports. European Xerox "asset-recovery" activity reports for 1992 indicate that the company reprocessed 50,000 field-returned copiers to yield 755,000 components (51% by weight), and recycled 46% by weight into reusable materials.

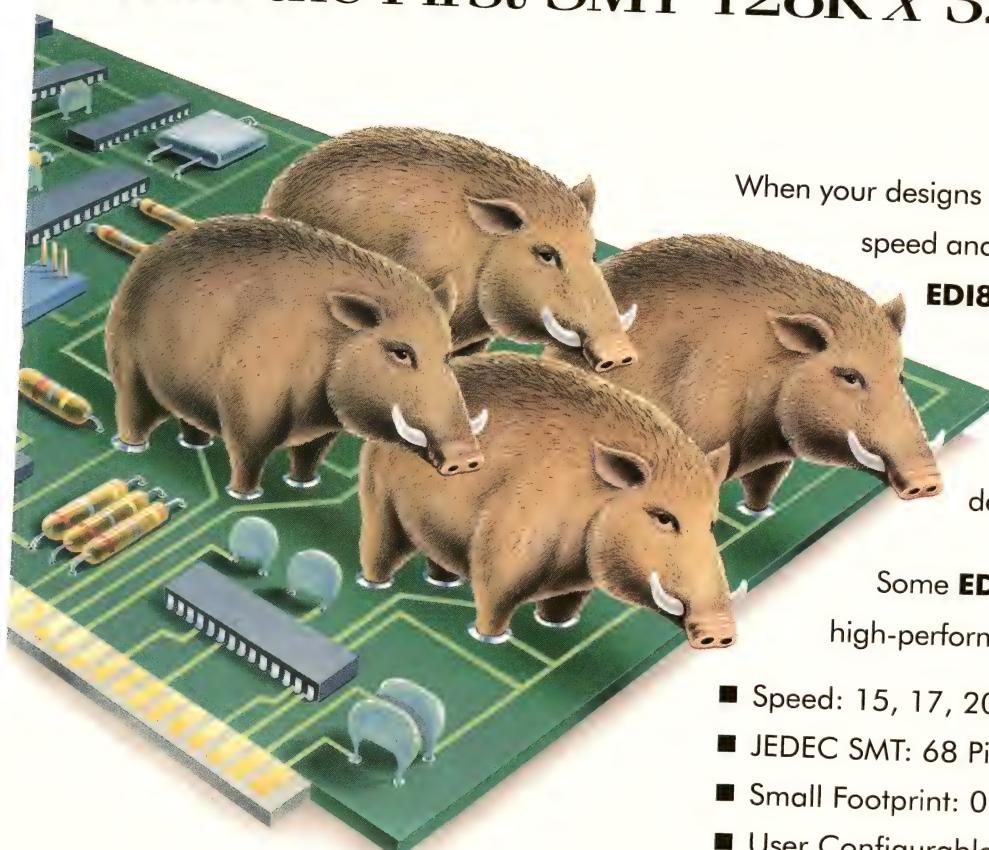
TABLE 2—ENVIRONMENTAL REQUIREMENTS

Product	Use/service	End-of-life management
Manufacture <ul style="list-style-type: none"> Materials should be recyclable (preferably on-site) • (plastic reground) — Maximize use of recyclable materials when environmentally preferable — Choose ODS-free components — Eliminate the use of toxic materials, such as Pb 	<ul style="list-style-type: none"> — Extend useful life through modular design with sufficient forward and backward capability — Make products upgradable <ul style="list-style-type: none"> • (ROM parts) • sockets for additional memory or processor chips) 	<ul style="list-style-type: none"> — Reuse parts (such as handsets and cords) — Standardize parts to facilitate remanufacture — Product components recyclable after consumer use — Open-loop recycling into fiber cables, spools, reels — Easy to disassemble: no rivets, glues, ultrasonic welding; minimal use of composites — Components easy to sort by marking and minimal use of materials — Housing should be shreddable
Process	Use/service	End-of-life management
Manufacture <ul style="list-style-type: none"> — Minimize process wastes, including air emissions, liquid effluents, and hazardous and nonhazardous solid wastes — Minimize resource and power consumption — Meet five corporate environmental goals — Do not commingle waste streams 	<ul style="list-style-type: none"> — Energy-efficient operation (operate on line power only) 	<ul style="list-style-type: none"> — Maximize material recycling of components not reused — Service or reconditioning operations should minimize use of paints and solvents — Minimize wastes, including air emissions, liquid effluents, and hazardous and nonhazardous solid wastes from refurbishing operations
Distribution	Use/service	End-of-life management
Manufacture <ul style="list-style-type: none"> — Minimize supplier packaging <ul style="list-style-type: none"> • (nonhazardous) — Packaging containing recycled material (postconsumer content specified) — Reusable trays for parts in factory 	<ul style="list-style-type: none"> — Minimize product packaging <ul style="list-style-type: none"> • (use Electronic Packaging Guidelines) • (nonhazardous inks, etc) — Optimize number of phones per package — Specify packaging containing recycled material (postconsumer content specified) — Use recycled paper for manual — Minimize material variety for packaging 	<ul style="list-style-type: none"> — Use reusable shipping containers — Use recyclable packaging — Use packaging containing recycled materials
Information management	Use/service	End-of-life management
Manufacture <ul style="list-style-type: none"> — Use design-for-environment (DFE) tools — Encourage suppliers to discontinue use of ODS in parts manufacturing 	<ul style="list-style-type: none"> — Print manual on recycled paper (list environmental features) — Print recycling instructions on product packaging 	<ul style="list-style-type: none"> — Supply toxic-material content — Provide product-recycling instructions — Provide product-disposal instructions

(Source: AT&T)

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CIRCLE NO. 122

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This left only 3% of the parts for disposal. Strategies to cope with end-of-life recovery point to a major paradigm shift for OEMs, according to Ray Dirby and Dewey Pitts of IBM (Research Triangle Park, NC). Designers must adopt upgradable modular-design approaches. Yvon Marty, Alcatel (France) points out that "recycling must be embedded into product design."

During the 1994 E and E Symposium, Thomas Porada of DEC called material recovery "asset alchemy." To recover valuable assets, the company has set two major programs, the Digital Idle Asset Listing (DIAL) and the Resource Recovery Center. Policy requires that departments should review DIAL before requesting new capital equipment. The policy has saved the company millions of dollars in equipment annually, says Porada. At the recovery center, DEC can sell recovered solid waste and process hazardous waste that the recovery processes generate. Without revealing quantities or dollar values, Porada describes DEC's own list of the six Rs: reuse (internally) 1.4% recovered; resale (equipment, components), 23.2%; refurbish, 1.4%; remanufacture, 0.3%; reclaim (printed wiring boards, ICs, cables, and connectors) 6.7%; recycle (metals, plastics, paper, and CRTs) 54.9%. Porada says the waste-to-energy conversion has been 12%. Hazardous landfill was less than 1%. Before disassembling materials, DEC carefully identifies proprietary components to prevent them from entering the market. Some high-value components are finding their way into toy markets via brokers, Porada says.

SHOULD WE RECYCLE OR DUMP BATTERIES?

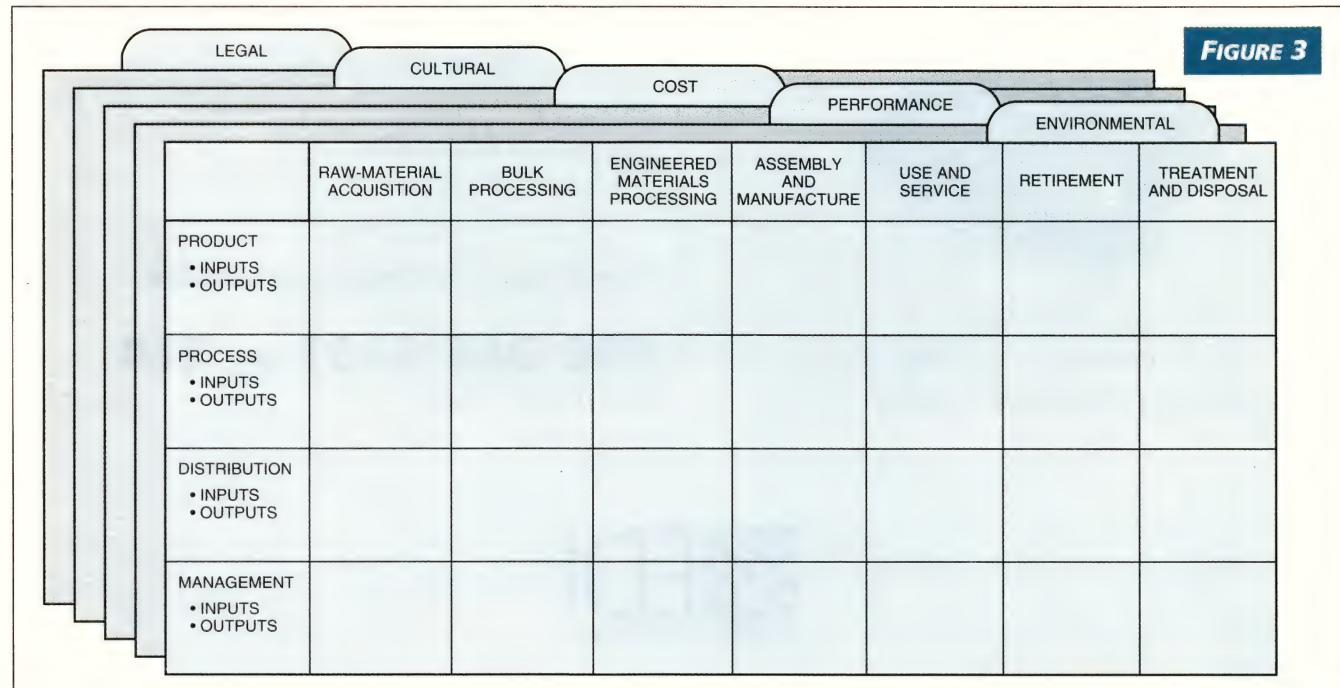
Every laptop computer user who discards dead batteries adds to the environmental problem. Of the dozen or so battery-cell types available, ranging from low specific energy (40 Whr/kg) to Lithium/polymer types (200 Whr/kg), all contain a high portion of toxic materials. Although government regulations prohibit putting lead-acid batteries into municipal waste, consumers regularly discard NiCd and nickel-metal hydride (NiMH) batteries, which are popular in laptops.

Because of the annual sales of 10 million portable computers, environmental engineers at Carnegie Mellon University, Pittsburgh, estimate that consumers will purchase 15 million battery packs annually, which represents 7700 tons of batteries. Assuming the replacement of two sets of batteries over a five-year period, that means we must dispose of 35 million units, or 17,500 tons, of toxic waste each year. Collections for household hazardous waste costs as much as \$10,000/ton, and bulk disposal of rechargeable batteries by the Department of Defense costs \$2000. Returning batteries to their manufacturer costs \$2/lb in shipping and handling plus a bulk-disposal fee, making the cost \$5000/ton.

Identifying all materials used is the key to easier recycling; all plastic parts must carry recycling symbols. Making parts from fewer material types and reducing paints, platings, and screws also aid in recycling. At Sony Europa (Fellbach, Germany), ideas for the reusability of electronic modules include more modularity and the storage of identification data within the module accessible through a so-called "green port." This data can also include life-history information for reuse decisions; identification ICs could store information about additives, fillers, and flame retardants in plastics, which hinder recycling.

Design for disassembly (DFD) will be a major requirement of DFE in applying the Six Rs as product take-backs increase. Researchers at Darmstadt University of Technology in Ger-

FIGURE 3



Conceptual-requirement matrices comprise tables of inputs and outputs vs manufacturing processes that affect them. (Source: EPA's *Life Cycle Design Guidance Manual*).

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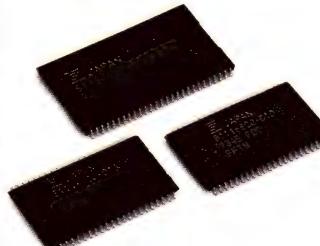
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many are exploring automatic disassembly of products through the use of a robot. Although they are still in the first stages of investigation, the researchers have accomplished complex disassembly. They are now investigating additional actuators and tools, and the next step is to integrate artificial-intelligence approaches. The Institute of Manufacturing Automation and Production Systems, Erlangen, Germany, is conducting longer term research that may lead to the analysis of printed wiring boards. The use of surface-mount components will win out over components with bent and soldered lead through holes, and companies will use adhesives less. Disassembly without destruction is the goal. **EDN**

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Author's biography

Jim Lippke is a managing partner of Sustainability Concepts, Solutions, a consulting company, where he has worked for three years. In his current position, he studies energy, economic, and employment issues and how to reduce energy usage and pollution. Jim has a BSEE from the University of Minnesota and is a member of the IEEE. He lists his main interest as being a mirror to the illuminating insights of others.

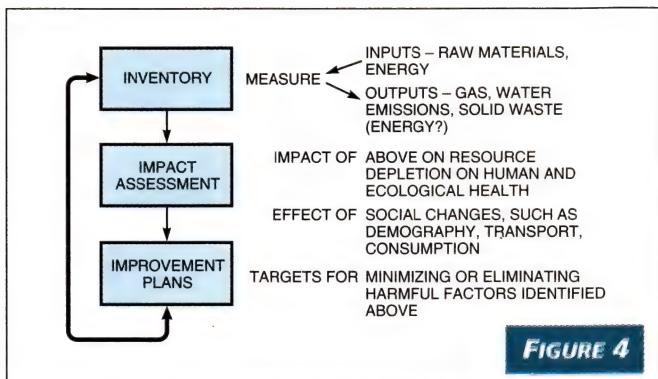


FIGURE 4

LCA comprises three interacting stages: inventory, impact assessment, and improvement plans. (Source: Ken Snowden, BNR Europe)

Acknowledgement

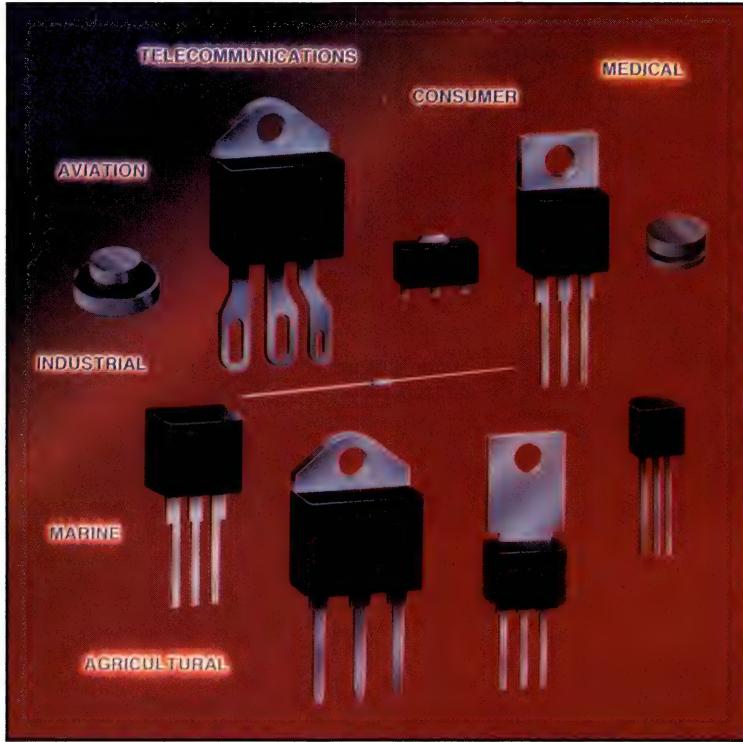
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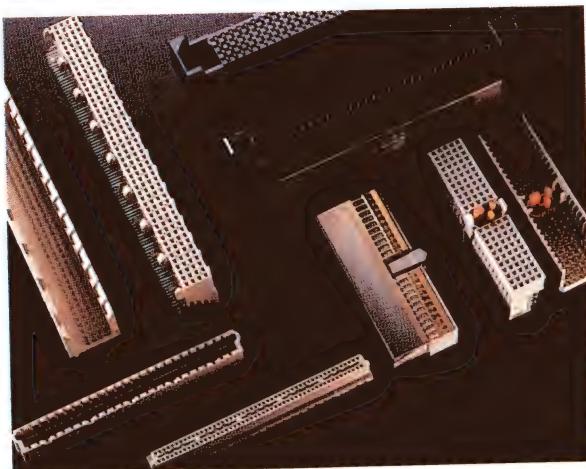
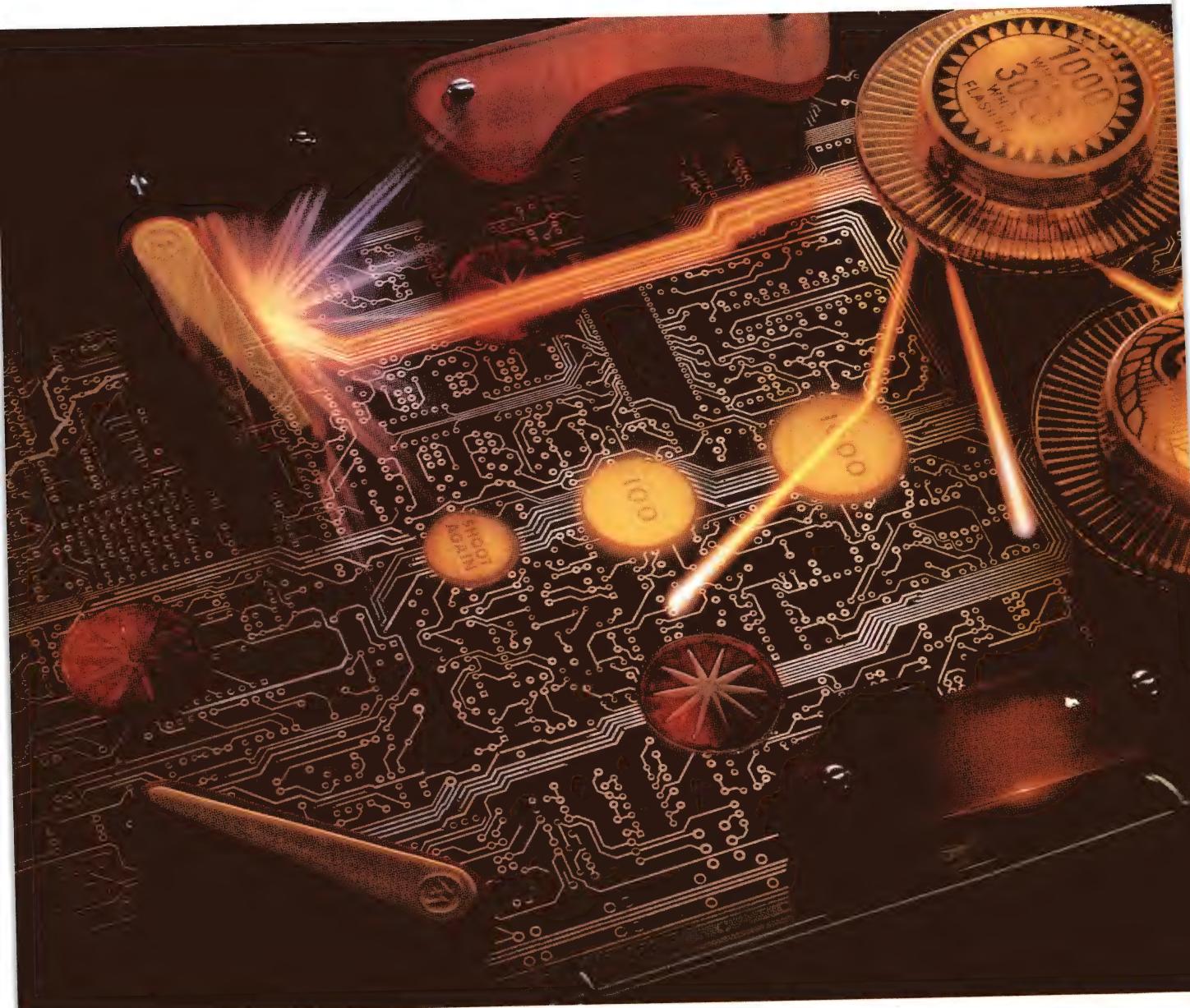
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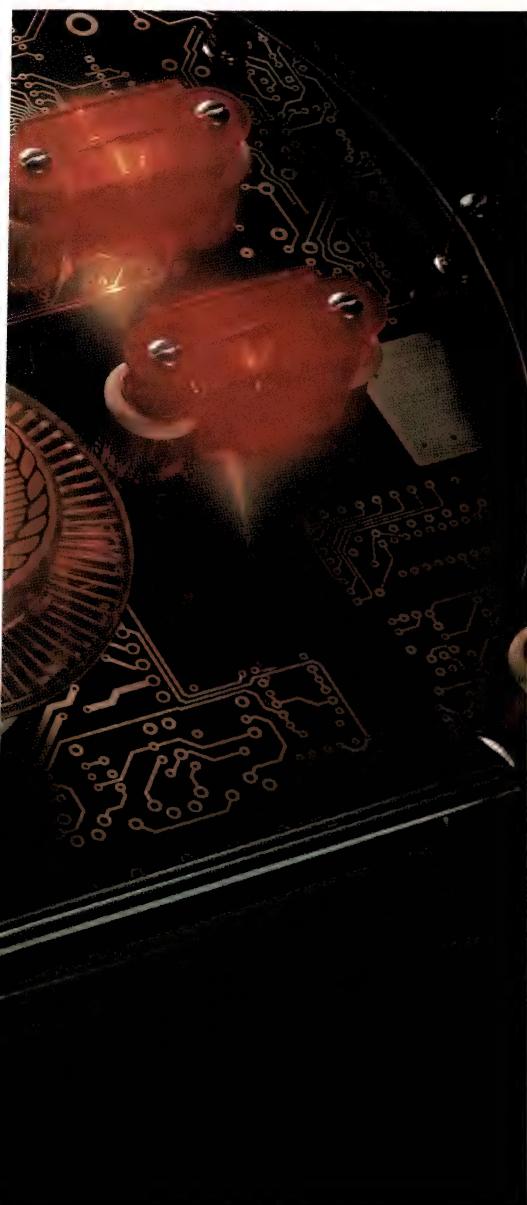
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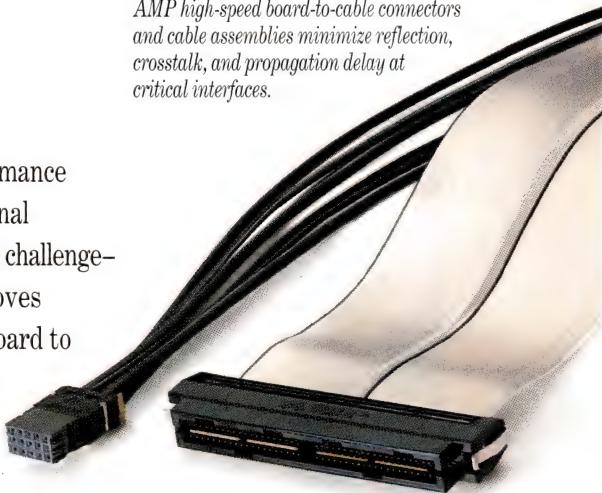


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The SAA7116 buffers each frame of the video capture chipset's digital output before burst-mode DMA-transferring it over the PCI-bus. These data transfers can be direct to the PC's video RAM for live display of the captured video, direct to a hard disk for storage, or via the computer's CPU so that the video image can be manipulated or compressed.

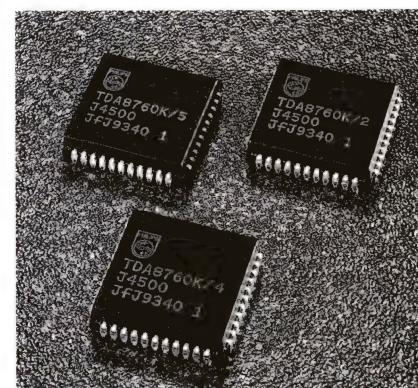
Typical applications for the SAA7116, when used in conjunction with the video capture chipset, include PC-based multimedia computers and PC-networked



The SAA7116 buffers and DMA-transfers the digital video data to any memory location on the PCI-bus at full resolution and frame rate.

distribution of real-time video sequences for education, training and information display.

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The TDA8760 10-bit A/D converter is available in three versions, with maximum sample rates of 20, 40 and 50 Msamples/s.

eliminate noise coupling between its analog and digital sections; separate multiple-pin analog and digital grounds prevent ground noise from affecting the digitization.

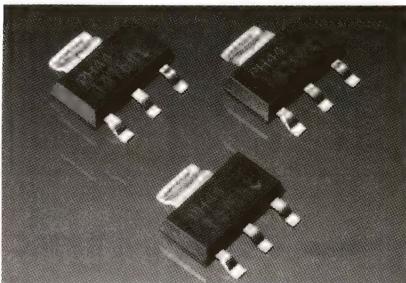
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SOT223-packaged power MOSFET has full on-chip protection

With the introduction of the BUK107 logic-level TOPFET, Philips Semiconductors is the first company to offer a temperature and overload protected 0.5 A low-side driver in a SOT223 surface-mount package. The BUK107 is designed primarily for lamp, solenoid and small motor switching in automotive applications such as engine management and driver information systems, but its built-in protection against short-circuit, over-temperature and over-voltage conditions also makes it suitable for a wide range of industrial applications where high reliability is required.

The transistor is available in two versions, either with a logic level control input that can be driven directly from a microcontroller port, or with a clamped input that can be used with a pull-up resistor drive circuit.



The BUK107 power MOSFET is the first fully-protected low-side driver to be offered in a true SMD package.

The BUK107 is a vertical DMOS power FET with an overload protection circuit that limits the drain current to typically 1 A, and an over-temperature protection circuit which senses the junction temperature to prevent thermal damage. In addition, integral overvoltage clamping diodes coupled with controlled turn-off of the FET limit the drain voltage to 50 V, allowing the BUK107 to be used for inductive load switching. No external protection components are required; all the active on-chip protection circuits are powered directly from the control input, so the BUK107 has an off-state current consumption of typically 1 μ A at 50 V. The device is housed in a standard SOT223 package with all pins protected against electrostatic discharges.

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Two new low-cost microcontrollers from 80C51-derivatives leader

With the introduction of the 8XC748 and 8XC749 8-bit microcontrollers, Philips Semiconductors continues to meet market demand for low-cost, small-memory-system microcontrollers. Both have a 16 MHz maximum clock frequency and 2 kbytes of program memory, while the 8XC749 also includes an on-chip A/D converter and PWM output so that it can perform analog I/O operations.

The 8XC748 and 8XC749 are targeted at a very broad spectrum of applications, ranging from toys and consumer products to industrial control and computing equipment. Their low power consumption and availability in SSOP packages make them particularly suitable for use in hand-held, battery-powered equipment. Philips Semiconductors is, in fact, the first company to offer 80C51-derivative devices in the miniature shrink small outline package.

Both microcontrollers are available in EPROM/OTP versions (87C748 and 87C749) and as mask-programmed versions



Philips Semiconductors' new low-cost microcontrollers are available in the miniature shrink small outline package (SSOP).

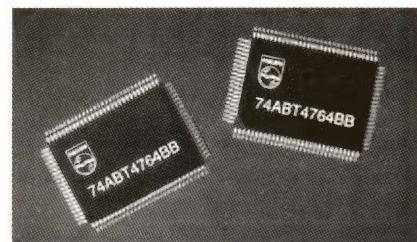
(83C748 and 83C749). Their 24-pin and 28-pin SSOP packages have a height of 2 mm and PC-board footprints of 66 mm² and 82.2 mm² respectively – less than half the mounting height and footprint of other surface-mount 80C51-derivative microcontrollers packaged in PLCCs. The new microcontrollers are also available in DIP and PLCC packages.

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First fully-programmable BiCMOS DRAM controller for high-speed, dual-port memory systems

Combining the efficiency of a standard dual-port DRAM controller with the flexibility of an application-specific device, the new 74ABT4764 features an 80 MHz on-chip PLD sequencer that can be programmed to control high-performance memory systems. In addition to operating with any type of DRAM, the 74ABT4764 has the ability to interface directly to CISC processors, RISC processors and DMA channels without the need for glue logic, and to arbitrate memory requests from any two of these devices and the memory's refresh logic.

Equipped with 16 CAS (column address strobe) outputs, four RAS (row address strobe) outputs and an on-chip multiplexer for 11-bit memory addresses, the 74ABT4764 directly addresses up to 4 Mbytes of memory. This can be made up from DRAMs with capacities up to 16 Mbit (4M x 4), and, with the addition of a few inexpensive logic chips, the device can



The 74ABT4764 fully-programmable BiCMOS DRAM controller offers exceptional flexibility.

also address 64 Mbit DRAMs. Memory access modes include page, fast page, interleaved page, nibble and static column modes, with datapaths up to 8 bytes wide.

The key to the 74ABT4764's exceptional flexibility is the on-chip PLD sequencer that controls the row/column address counters and multiplexer, the loop counter and an active page comparator that detects whether the current row address is within an active memory page. The counter overflow outputs and the hit/miss output of the active page comparator all feed back to the sequencer inputs.

The 74ABT4764 is manufactured in Philips' QUBIC BiCMOS process.

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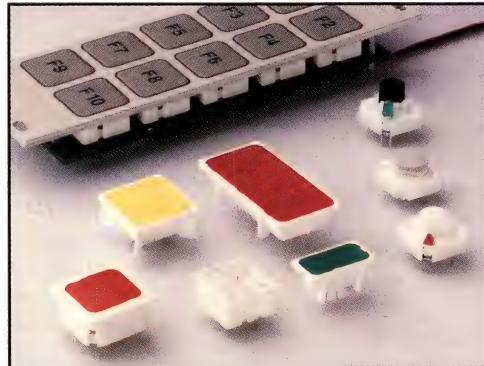
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The RF15/19 modules are available with various actuator heights (6.2–22.5mm) and with spot and full integral illumination using red, green or yellow LEDs. The individual RF15/19 modules are assembled robotically for consistent, high quality and all have outstanding tactile feel with operation life in excess of one million actuations.

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Secondary cache increases performance and reduces power use in portable PCs

J THOMAS PAWLICKI, MICRON SEMICONDUCTOR INC

Secondary SRAM cache can increase system performance and reduce power consumption in portable PCs by varying degrees, depending on the system configuration. Copying a portion of main memory into fast SRAM increases the system speed by reducing the number of accesses to slower DRAM. System-design choices affect the cache efficiency and determine power consumption and performance. The choice of hardware and architecture that optimizes one software application may have a negative impact on other applications.

A performance and power analysis comparing the effect of cache on system designs can demonstrate the value of architectural choices. Although the variety and complexity of μ Ps, chip sets, and operating systems (OSs) make analysis difficult, the following example can provide an indicative comparison.

Performance and power analysis parameters

Our analysis employs a 486SX-33 with 4 Mbytes of DRAM, a common main-memory configuration. You can use 3.3V SRAM with 5V-tolerant inputs and outputs or 5V SRAMs when adding an external cache to a 5V CPU. Because the CPU is buffered from main DRAM, you can use 5 or 3.3V DRAMs with 3.3V CPUs. The analysis includes several combinations of cache and main memory to investigate the alternatives' sensitivity to supply voltage, cache-SRAM type, assumed internal and external cache-miss rates, and DRAM type.

At 33 MHz, a 5V 486SX μ P running at full speed uses 685 mA of current. This figure includes a margin for high supply voltage, low operating temperature, and test guard band. Typical μ P operation requires 15% less current than specified (590 mA). Only a small portion of the CPU circuitry draws

For some time, the main focus of portable-computer development has been to extend the computer's operating time on a single battery charge. Performance considerations were secondary. However, now that portable operation ranges to eight hours plus, the focus is shifting toward improving operating performance. The new challenge is to improve operating speed without sacrificing the gains in mobile operation time.

less power when a wait state occurs on the μ P's external bus. When the bus-execution unit idles during a wait state, the 486SX μ P's five-stage internal pipeline (instruction fetch, two decode stages, execution, and register write-back) is still active. We calculate a 15% reduction in energy consumption during wait states because no more than two or three wait states occurs per bus cycle. The power reduction can be greater for a design that invokes more wait states.

The mix of bus-cycle operations varies widely with software applications and OSs. Determine a reasonable, nominal bus-cycle mix to evaluate hardware performance for your application. In our spreadsheet analysis (Table 2), we compare the bus-cycle mix and Level 1 cache-miss rates for each hardware alternative to determine μ P performance and energy use. We determine sensitivity to the bus-cycle mix and the selected average miss rate by evaluating the alternatives and increasing and decreasing the miss-rate value. Similarly, you can evaluate sensitivity to the average bus mix by altering the ratio between reads and writes.

We evaluated performance for each alternative by calculating the number of elapsed clock cycles to execute 1 billion operations. An operation is an instruction fetch/execution cycle or a data read/write cycle. Given the bus-cycle mix, we select memory speeds and then determine the number of wait states for each bus-access type. Although wait states reduce the power consumption per cycle, they add to a task's overall execution time.

Ideally, a system should execute the selected operations in 1 billion clock cycles. The memory architecture imposes wait states that cause the number of clock cycles to complete the

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task to exceed 1 billion cycles.

It is difficult to determine power consumption in CMOS circuits because transistors use energy when they are toggled and leak energy when they are not toggled. Consequently, we use many analysis methods to calculate the instantaneous peak power of the components and use this figure to evaluate energy use. This method can be misleading because a component that consumes more peak power can use less energy overall. Although power dissipation is the rate of energy use, power consumption is $power \times time$. A good analysis evaluates standby power multiplied by the standby time in addition to active power multiplied by the active time.

Also, a peak-power calculation alone does not account for I/O energy use. Although manufacturers specify operating current with no loading on devices' outputs, ICs in the real world drive capacitive loads, and it takes energy to alter the voltage of the load capacitance. Take the load energy (calculated as $\frac{1}{2} CV^2$) into account in analyzing power consumption.

The four types of DRAM refresh that can affect a system's power consumption are: standard, extended, self-refresh, and pseudostatic. Manufacturers screen DRAMs to find chips that can hold data for long times between refresh cycles. These "extended-refresh" devices use less standby power. Our analysis uses the conventional, standard-refresh DRAM and extended-refresh devices. Self-refresh DRAMs do not need an external clock to continue refreshing the device so the DRAM controller can cease operation when the system is idle, reducing power dissipation. Pseudostatic RAMs are similar to the self-refresh devices, except the pseudostatic devices' address rows and columns are not multiplexed. Both the self-refresh and pseudostatic DRAMs are not yet widely available, and pseudostatic RAMs have not successfully penetrated the PC market. Therefore, we omit these products in our study.

In a simple design, a secondary cache subsystem adds approximately 2000 to 4000 gate equivalents to a chip set. A DRAM controller uses 1000 to 2000 gates. These gates consume energy at the rate of $6 \mu W/MHz/gate$ in a 5V gate array and $4 \mu W/MHz/gate$ in a 3.3V gate array. When a system is in standby

mode, gates do not truly operate at zero power. You observe zero-power operation only if you stop the clock to the gate. Therefore, our analysis includes power consumption values of $0.3 \mu W/5V$ gate and $0.2 \mu W/3.3V$ gate in standby mode.

One difficulty of a performance and power analysis is determining how

seventh groups (cases 18 and 19 and 20 and 21, respectively) examine the effect of using extended-refresh DRAM in both 5 and 3.3V systems.

The last two columns of **Table 2** show figure-of-merit improvements (if any) over the baseline case (Case 1). The next-to-last column in **Table 2** shows improvement over Case 1 for the

TABLE 1—POWER DISSIPATION FOR SYSTEM COMPONENTS

Device	Supply voltage (V)	Active power (mW)	Standby power (mW)	Power dissipation (Clock stopped, mW)
DRAM controller	5	60	30	10
DRAM controller	3.3	40	20	5
Cache controller	5	200	60	0.6
Cache controller	3.3	135	40	0.4

many gates run at which frequencies. If the chip-set vendor cannot supply accurate data, you can assume power dissipation based on the device's data-sheet maximum currents for each operating mode. If you use such an assumption, you can test sensitivity by adjusting the numbers up and down in the spreadsheet model to establish the affected range.

Table 1 shows the power-dissipation data in our analysis. The DRAM controller's clock-stopped numbers assume some dynamic operation when the CPU goes idle to account for DRAM-refresh requirements. The power data does not include additional components in chip sets such as I/O control.

Analysis results

Table 2 lists the results of the 21 design options we consider in our analysis. Case 1 is the reference or base case. The **table** divides the cases into seven major groups. The first group (cases 1 through 6) employs variations based around a 5V CPU and 5V DRAM. The second group (cases 7 and 8) also uses 5V DRAM but substitutes a 3.3V CPU. The third group (cases 9, 10, and 11) employs both a 3.3V CPU and 3.3V DRAM.

The fourth group (cases 12 through 14), employs a 5V CPU and DRAM, but we threw high cache miss rates into the simulation to test for sensitivity. The fifth group (cases 15 through 17) also looks for that sensitivity, using a 3.3V CPU and 3.3V DRAM. The sixth and

first case of each of the seven groups. The last column in the **table** shows additional incremental improvements achieved by modifying the configuration of the first case in that group.

In each case, we execute an application consisting of 1 billion clock cycles followed by a 5-minute idle period. This scenario assumes a 90% idle time for mobile-computer operation. A more realistic idle time is 70 to 85%. We use the more conservative model because the addition of components increases standby power needs. If the addition of Level 2 (secondary) cache shows benefits in worst-case scenarios, then we can project its efficiency in less extreme conditions.

For all cases, except where indicated, we halted the clock after 60 sec of idle time to emulate some power management. The final 4 minutes of operation were in the lowest energy consumption mode (rather than off). The figure of merit that compares the options is

$1 \times 10_9 \text{ operations}/(\text{CPU and memory subsystem energy} * \text{execution time})$.

Larger figures of merit indicate better performance using less power. Cases with SRAM secondary cache, one additional 32k \times 8-bit SRAM, include a tag RAM in the energy calculation at the same voltage as the cache SRAM. For example, in Case 6, the energy figures include one additional 3.3V, 32k \times 8-bit SRAM acting as a tag RAM. This is nec-

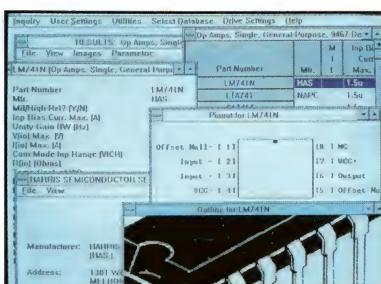
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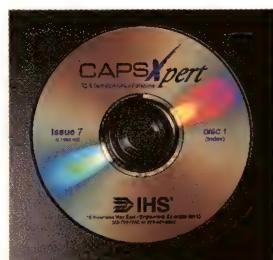
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essary because Table 1 doesn't account for the tag.

Table 2 clearly shows the importance of stopping the clock. You incur a 24% energy penalty if the clock runs continuously rather than stopping after 60 sec of idle time. All components use more energy when the clock is running. Restarting the CPU and core devices requires less time and energy than spinning a hard disk drive up to speed.

The table shows a 9.6% improvement

in the figure of merit when you add a 5V secondary cache (four, 32k×8-bit SRAMs for cache data, and one 32k×8-bit SRAM for cache tag) to a 5V system. Although the power consumption is higher in standby mode, active energy consumption is considerably lower. In this case, the performance improvement outweighs the overall energy increase. In comparing cases 4 and 2 (with clock running), an overall decrease in the figure of merit appears

when you add cache (Case 4). This further emphasizes the need to control the system clock.

In cases 5 and 6, the secondary cache employs 3.3V devices. Case 5 uses four 32k×8-bit SRAMs for the data cache, and Case 6 uses a 32k×32-bit synchronous-burst SRAM. Both cache configurations employ 5V-tolerant parts. These ICs run on a 3.3V supply, but they don't require buffering to interface directly with the 5V CPU. These two cases show

TABLE 2—SPREADSHEET RESULT OF POWER SIMULATIONS

Case No.	Option	Elapsed times	Active-period energy (J)	Standby-period energy, excluding CPU (J)	Standby period energy (J)	T = total time
1	5V DRAM	38.388	205.6	18.822	303.8	338.388
2	5V DRAM, clock always running	38.388	205.6	24.882	467.4	338.388
3	5V CPU, 5V DRAM, four 5V 32k×8-bit cache RAMs	31.421	142	47.466	332.5	331.421
4	5V CPU, 5V DRAM, four 5V 32k×8-bit cache RAMs, clock always running	31.421	142	147.82	590.3	331.421
5	5V CPU, 5V DRAM, four 3.3V 32k×8-bit cache RAMs	31.421	126.9	31.476	316.5	331.421
6	5V CPU, 5V DRAM, one 3.3V 32k×32-bit cache RAM	31.421	124.9	30.288	315.3	331.421
7	3.3V CPU, 5V DRAM	38.388	143.9	18.822	137	338.388
8	3.3V CPU, 5V DRAM, 3.3V 32k×32-bit cache RAM, 3.3V cache controller	31.421	71.7	29.04	147.2	331.421
9	3.3V CPU, 3.3V DRAM	38.388	89.2	7.6789	125.9	338.388
10	3.3V CPU, 3.3V DRAM, 3.3V 32k×32-bit cache RAM	31.421	61.1	17.897	136.1	331.421
11	3.3V CPU, 3.3V DRAM, four 32k×8-bit cache RAMs	31.421	62.9	19.085	137.3	331.421
12	5V CPU, 5V DRAM, high miss rates	46.776	263.5	18.822	303.8	346.776
13	5V CPU, 5V DRAM, high miss rates, four 3.3V 32k×8-bit cache RAMs	32.842	157.2	31.476	316.5	332.842
14	5V CPU, 5V DRAM, high miss rates, 3.3V 32k×32-bit cache RAM	32.842	154.2	30.288	315.3	332.842
15	3.3V CPU, 3.3V DRAM, high miss rates	46.776	114.3	7.6789	125.9	346.776
16	3.3V CPU, 3.3V DRAM, high miss rates, four 3.3V 32k×8-bit cache RAMs	32.842	78.5	19.085	137.3	332.842
17	3.3V CPU, 3.3V DRAM, high miss rates, 3.3V 32k×32-bit cache RAM	32.842	75.8	17.897	136.1	332.842
18	5V CPU, 5V extended-refresh DRAM	38.388	204.6	5.6762	290.7	338.388
19	5V CPU, 5V extended-refresh DRAM, 32k×32-bit cache RAM	31.421	123.6	17.142	302.1	331.421
20	3.3V CPU, 3.3V extended-refresh DRAM	38.388	88.8	2.6712	120.9	338.388
21	3.3V CPU, 3.3V extended-refresh DRAM, 32k×32-bit cache RAM	31.421	60.9	15.544	133.7	331.421

considerably improved figures of merit. This analysis presumes the availability of a 3.3V tap from the switch-mode power supply so no additional energy is allocated to convert 5 to 3.3V. If a 3.3V power-supply tap is not available, take the additional power requirements of a linear regulator into account.

During operation and in standby mode, the single 32k×32-bit SRAM-based secondary cache uses slightly less energy than the cache built from four

32k×8-bit SRAMs. One additional consideration in this case is the circuit-board design. The single 32k×32-bit SRAM in a TQFP uses 0.55 in.² of board space, and the four 32k×8-bit devices, packaged in SOJ packages, use 1.1 in.². This reduction in real-estate consumption can make a significant difference to a crowded circuit board, especially in mobile computers.

Cases 7 and 8 reflect some of today's harsh market realities. Low-voltage

CPUs really need the more energy-efficient 3.3V DRAMs, but these memories are still in short supply. Thus, cases 7 and 8 reflect the results of using a 3.3V CPU with 5V DRAM. Case 7 (3.3V CPU without a secondary cache) shows an improvement of 81% over the 5V CPU design. Adding a 3.3V secondary cache further improves this design by 31%.

In cases 9 through 11, the cache, CPU, controllers, and DRAM all run on 3.3V. Thus, as 3.3V DRAMs become more available and less costly, all-3.3V systems should dominate system designs.

Cases 12 through 17 illustrate sensitivity analysis. When you make a set of assumptions, check your conclusions' sensitivity to those assumptions. We developed a set of miss rates for levels 1 and 2 caches and applied these rates against the original bus-cycle mix (which comprises 11% internal cycles, 52% instruction-read cycles, 21% data-read cycles, and 16% data-write cycles). Each of the three internal bus-cycle operations (Level 1 cache operations) uses different miss rates.

When you add Level 2 cache, the 128-kbyte direct-mapped cache uses a set of miss rates that conforms to an average rate that falls between DOS' and Windows' typical miss rates. Windows is more sensitive to miss rates than is DOS. To determine the power-consumption sensitivity to miss rates, cases 12 through 17 use miss rates in levels 1 and 2 caches that are twice as high as those of the other cases. This doubling more closely resembles a true Windows operating environment. Level 2 caches improve the computed figures of merit by 16% to 26%, depending on CPU and DRAM voltage selections.

The last group of options in Table 2 explores an effort to reduce DRAM energy in the cacheless cases through the use of extended-refresh DRAMs. Extended-refresh DRAMs have lower standby energy demands because they need refreshing much less often than regular DRAMs. If any of the cases casts doubt upon the usefulness of Level 2 cache, it would be these because we figure a high standby time into the analysis. But even in this scenario, adding the secondary cache improves the figures of merit from 10 to 19%.

The 33-MHz, 486-μP-based portable computer hardly represents a performance pinnacle. Clock-doubling and -

E= total energy (J)	Figure of merit (1E9/(E*T))	Improvement over baseline case (%)	Incremental improvement (%)
509.4	5801	Baseline	
673	4391		-24.303
474.5	6359		9.622
732.3	4120		-28.975
443.3	6806		17.327
440.1	6855		18.177
280.9	10521	81.362	
218.9	13780		30.983
215.1	13738	136.827	
197.2	15302	11.38	
200.1	15075	9.733	
567.3	5083	-12.38	
473.7	6343		24.794
469.5	6399		25.891
240.2	12005	-12.613	
215.7	13927		16.001
211.9	14179		18.104
495.3	5966	2.850	
425.7	7088		18.802
209.7	14093	2.582	
194.6	15504		10.010

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tripling μ Ps are finding their way into the portable-computing market. However, a μ P consumes energy when executing instructions and when waiting. During wait states, the μ P performs no useful work, but it consumes 80 to 85% of the energy it normally uses during full operation. Each bus wait state in a clock-tripled system corresponds to three internal wait states in the CPU. Although the μ P performs no work, it still needs 80% of the active energy for each of these three wait-state cycles. Unless you add secondary cache to the number of wait states, the clock tripling reduces the system's overall energy efficiency. Therefore, adding Level 2 cache improves the efficiency of clock-doubled and -tripled systems even more than it does in unity-clock systems.

Core mobile-computer systems will soon include Level 2 cache because of the performance advantages it brings. IC vendors will most likely integrate tag SRAM into chip sets to save board space. Although tag RAMs integrated into ASICs have lower performance than external specialty tag SRAMs, portable computers usually do not need to perform at workstation levels, so you can achieve zero-wait-state results with ASIC-based tag RAMs. Thus, a single 3.3V 32k \times 32-bit SRAM would be the most likely choice for the Level 2 cache RAM because it requires the least amount of circuit-board space. **EDN**

Author's biography

J Thomas Pawlowski is strategic SRAM applications engineer at Micron Semiconductor Inc in Boise, ID. He has worked at Micron for 2½ years. In his current position, he architects new products and assists customers and engineers with design activities. Pawlowski has also helped develop SyncBurst SRAM, PCs, and aerospace embedded-control systems. He received a BSEE from the University of Waterloo, Waterloo, ON, Canada. In his spare time, Pawlowski enjoys scuba diving, high-performance car design, music, and studying the philosophy of religion.

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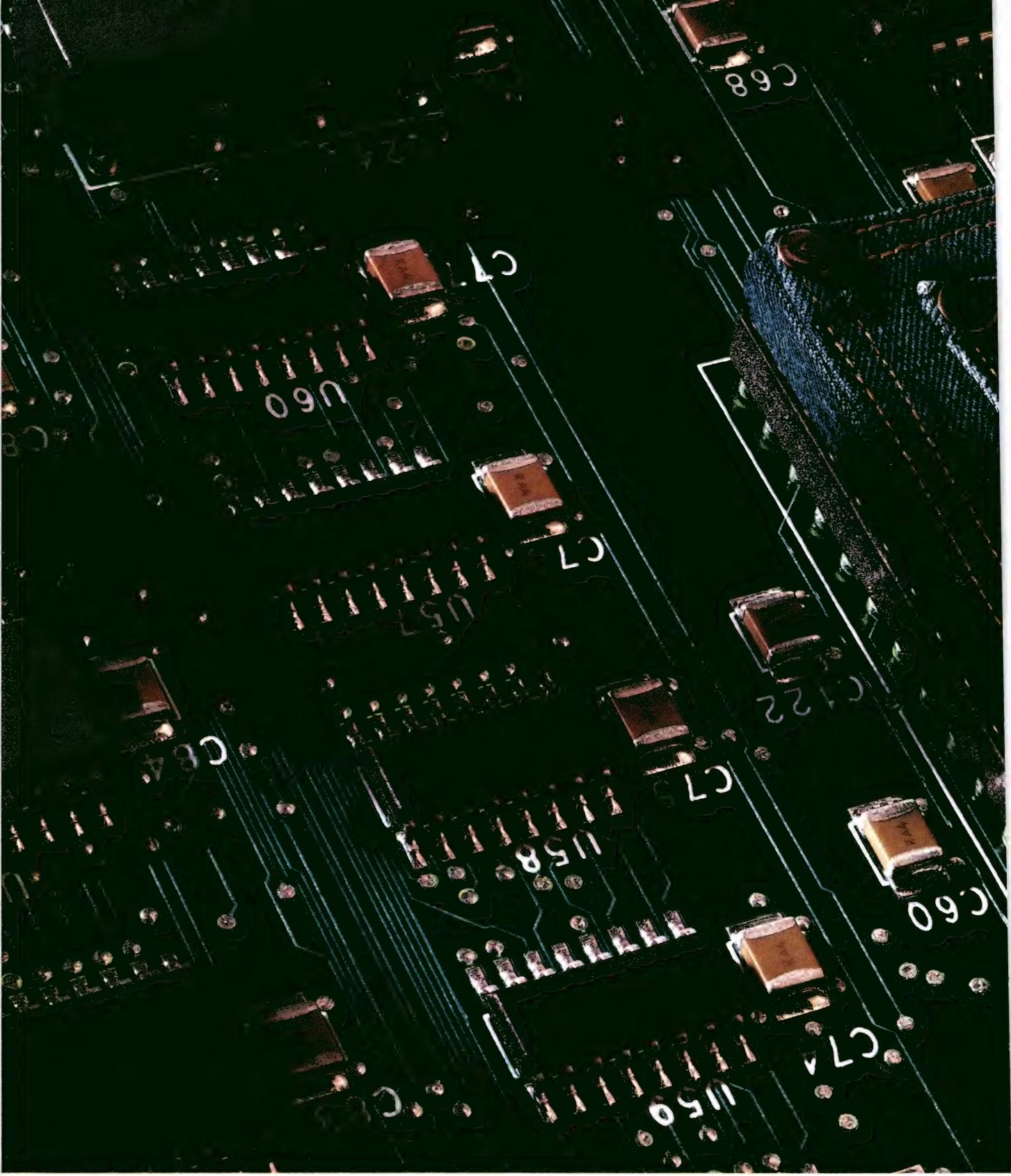
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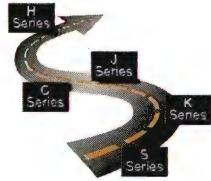
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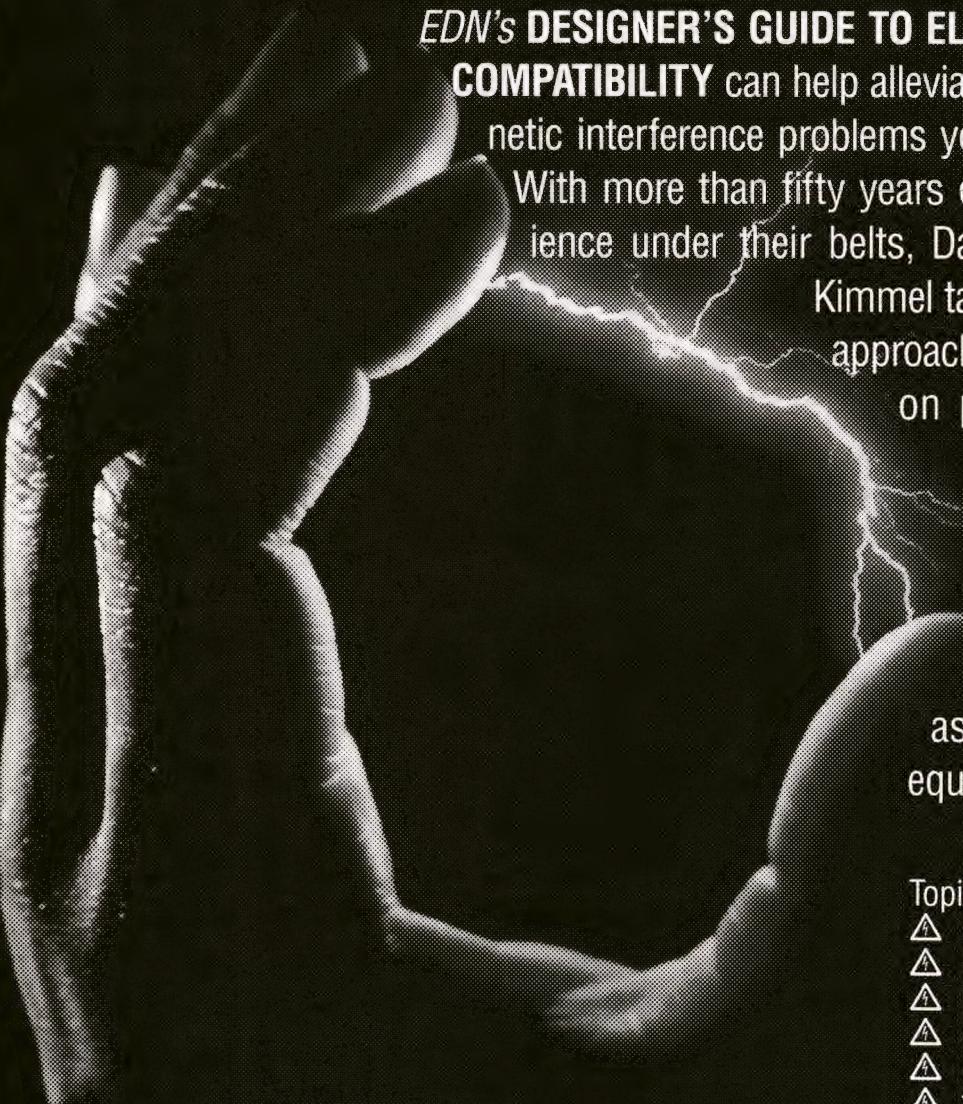
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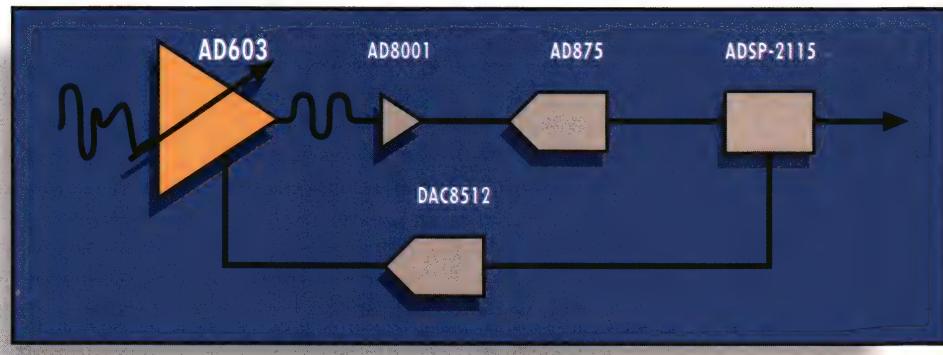
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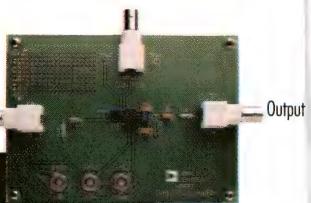
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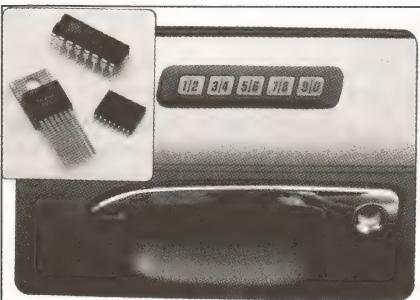
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RAMDAC provides 64-bit video interface. The TVP3025 RAMDAC provides a complete back-end graphic system by interfacing a graphic controller device directly to VRAM. The device operates at speeds of 135, 175, or 220, providing 24-bit true color at 1024×768 resolution and 16-bit color at up to 1600×1280 resolution. The TVP3025-135PCE costs \$23.75 (1000). **Texas Instruments Inc**, Denver, CO. (800) 477-8924 ext 4500. **Circle No. 382**



Multifunction linear-voltage regulator extends battery life. The CS-8151 linear-regulator IC provides a single 5V regulated output with a 100-mA current capability to power a microprocessor. A single external capacitor sets the reset-pulse width, wake-up frequency, and reset-to-wake-up delay time. A wake-up pulse train periodically activates a μ P to check for service requests. If the μ P does not respond to the wake-up pulse, the device issues a reset signal. \$1.56 (10,000). **Cherry Semiconductor Corp**, East Greenwich, RI. (401) 885-3600. **Circle No. 383**

Embedded-system controller works with IDT's R3051 32-bit RISC CPU. The GT-32011 provides a tightly coupled CPU interface; a DMA interface for an external coprocessor; a ROM controller for up to 20 Mbytes; a high-performance DRAM controller for up to 40 Mbytes; a fully compliant IEEE 1284 bidirectional Centronics interface; three high-performance DMA channels, a 16-bit I/O bus, an I/O controller with various DMA, packing, and unpacking features; a 24-bit timer/counter; and other functions. \$17.95 (10,000). **Galileo Technology Inc**, San Jose, CA. (408) 451-1400. **Circle No. 384**

Single-chip SCSI designed for fast and low-cost SCSI-2 PCI adapter boards.

According to the company, the \$19.95 (1000) AM53C974A allows companies to quickly develop SCSI adapters at low cost. In addition to the chip, the company provides complete licensable SCSI software, an FCC-tested reference platform, and complete design support. The chip contains a fast SCSI-2 core, bus-master DMA engine, and PCI-Bus interface unit. Automatic SCSI device assignment provides Plug-and-Play compatibility, sampling now. **Advanced Micro Devices Inc**, Sunnyvale, CA. (408) 732-2400. **Circle No. 385**

16-bit delta-sigma ADC converts 192 ksamples/sec.

The ADC16471 \$11.50 (1000) with internal-voltage reference and the 16071 \$11.10 (1000) requiring an external-voltage reference have adjustable throughput rates of 7 to 192 ksamples/sec. The converters include a fourth-order modulator, provide 64 times oversampling, and include a linear-phase digital antialiasing filter. The device dissipates 500 mW at the maximum sample rate and has a 6.5 mW power-down mode. **National Semiconductor Corp**, Santa Clara, CA. (800) 272-9959. **Circle No. 386**

Variable gain-control circuit on single IC.

The EL4451C variable-gain amplifier has a 70-MHz bandwidth, a gain of two, and attenuation greater than 70 dB at 4 MHz. The bipolar IC operates on power supplies from ± 5 to ± 15 V and has an analog-input range of ± 2 V. The IC is designed for variable filters, level controls, and automatic gain controls. Available in 14-pin P-DIP and 14-lead SO packages, from \$3.33 (1000). **Elantec Inc**, Milpitas, CA. (408) 945-1323. **Circle No. 387**

Positive-to-negative dc-to-dc converter has 1.5 to 15V range.

The TC7662B converter has an operating current of 80 μ A and requires two external capacitors. The device can also be connected to function as a voltage doubler, multiplier, or divider. Available in an 8-pin DIP or SOIC package. \$0.88 (1000). **Telcom Semiconductor Inc**, Mountain View, CA. (415) 968-9241. **Circle No. 388**

Complete current-sensing IC includes sense resistor in 8-pin SO package. The MAX471 uses an inter-

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nal 35-mΩ resistor that measures battery currents up to ±3A with accuracy to 2%. The IC operates from 3 to 6V and draws less than 100 μA. The MAX472 uses an external resistor for applications requiring higher current or greater precision at low current levels. From \$1.90 (1000). **Maxim Integrated Products**, Sunnyvale, CA. (408) 737-7600 ext 6087.

Circle No. 389

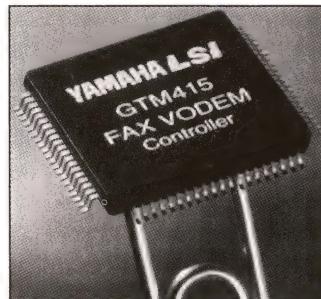
20-bit delta-sigma ADC has 110-dB dynamic range. The CS5390 generates a 20-bit value for two channels in serial form and samples at up to 50 kHz per channel. The converter uses a 64-times oversampled, fifth-order modulator to achieve its wide dynamic range. An on-chip digital antialiasing filter reduces external filter requirements to a single external RC filter per channel. The CS5390 is

packaged in a 28-pin DIP and costs \$58 (1000). **Crystal Semiconductor Corp.**, Austin, TX. (512) 422-7555.

Circle No. 390

in an 80-pin QFP or TQFP, the IC costs \$11 (1000). **Yamaha Systems Technology Division**, San Jose, CA. (408) 437-3133.

Circle No. 391



Fax vodem controller operates on 3.3V. The GTM415 replaces the GTM407 with new features and the ability to operate from 3.3, 5, or mixed-voltage systems. The new device offers higher speed and an improved baud-rate generator and controls the fax, voice, data, and caller-identification functions. Packaged

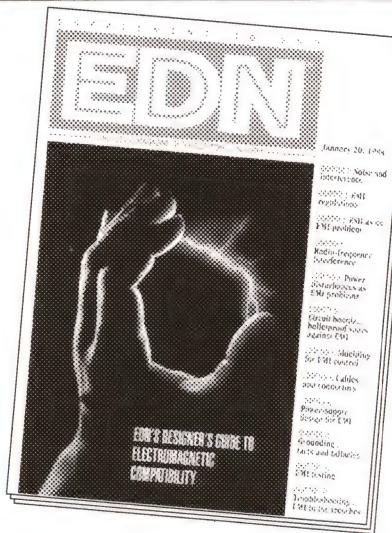
Dc-to-dc converter minimizes RF interference in portable communication products. The TK6501S provides a 3V regulated output at up to 15 mA from input voltages as low as 0.9V. The IC issues a reset signal if the output falls below 2.4V. Low switching transients and a laser-trimmed internal oscillator minimize interference for communication systems using a 455-kHz IF. \$1.40 (1000). **Toko America Inc.**, Mt Prospect, IL. (708) 297-0070. **Circle No. 392**

Two-chip set for PCMCIA flash-memory cards. The CL-ST1000 PCMCIA/ATA flash-memory controller and

CL-ST2000 space manager simplify the creation of flash memory-based storage systems that emulate rotating magnetic hard disk drives. The chips are available with a storage-card-reference design to reduce the time and cost of developing flash-memory cards. You can create a 2-Mbyte flash-storage card using the CL-ST1000, an 8-bit μP, and a flash-memory chip. Creating larger flash-storage cards also requires the use of the CLS-ST2000 space manager. Samples of both chips will be available in the fourth quarter. \$22 (1000). **Cirrus Logic Inc.**, Fremont, CA. (510) 226-2147. **Circle No. 393**

Fast-charge IC for NiMH and NiCd batteries features peak-voltage detection. The bq2002 has peak-voltage detection for fast-charge termination of NiMH batteries. The charger

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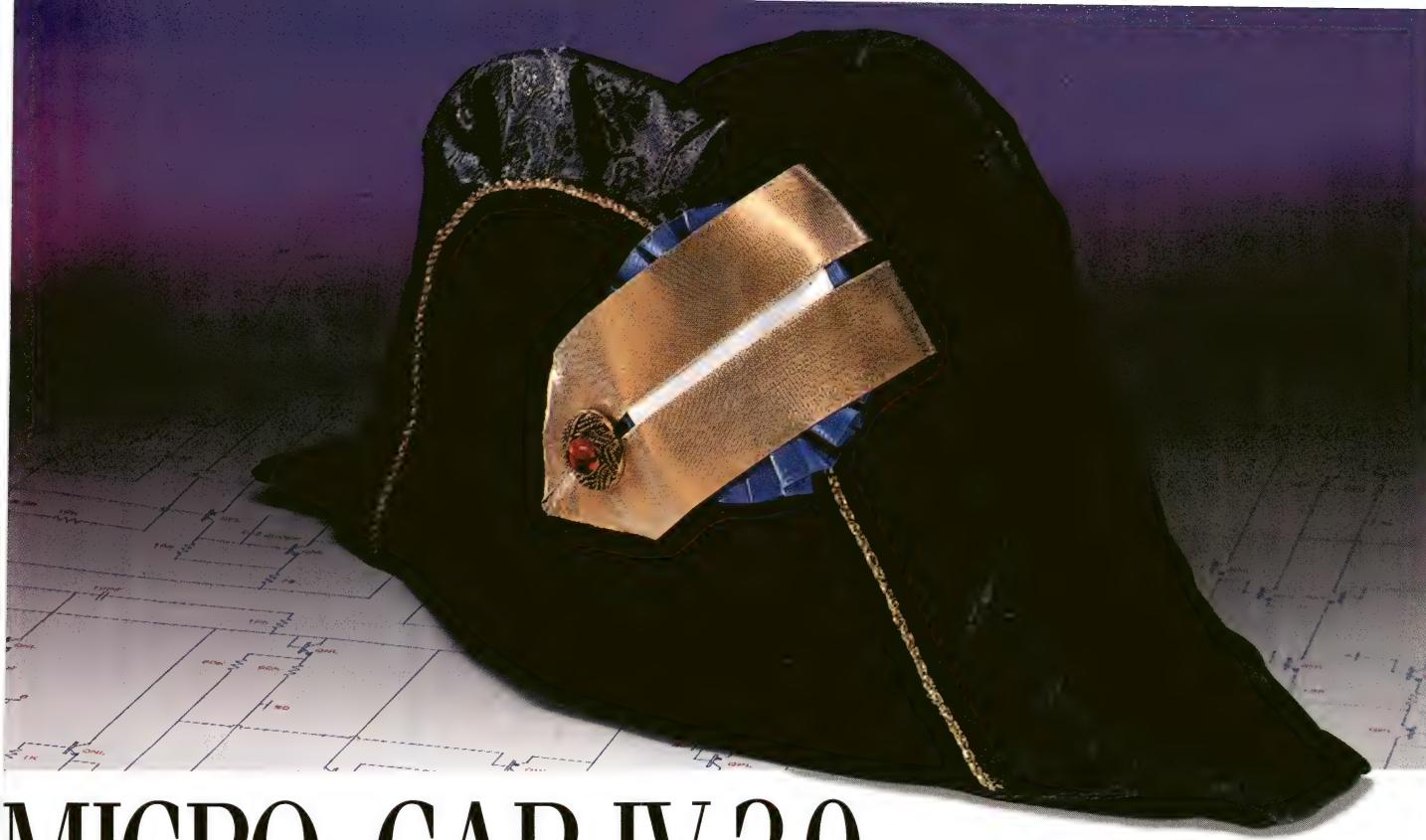
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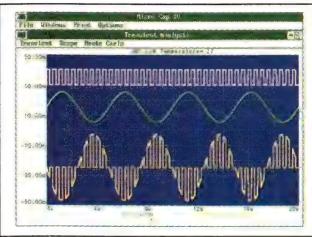


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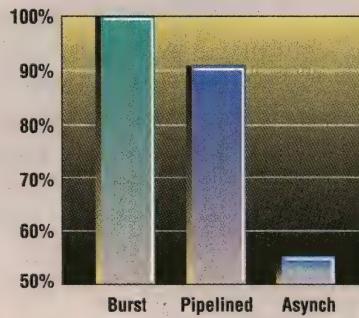
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also terminates charge based on negative-delta voltage detection for NiCd batteries. Fail-safe terminations include maximum temperature and maximum charge time. Other features include a charge-inhibit pin to temporarily disable fast charge, a low-power standby mode, battery-temperature and voltage qualification before fast charge, and pulse-trickle and top-off charge control. \$1.45 (5000). Development systems are \$75. **Benchmarq Microelectronics Inc**, Carrollton, TX. (214) 407-0011.

Circle No. 394

Converter for battery-operated systems has low-battery detector and up to 88% efficiency. The LT1303 dc/dc converter is available in a fixed 5V, 200-mA version and an adjustable-output version that delivers up to 25V. The converter operates on 1.8 to 5V, with typical conversion efficiencies ranging from 80 to 88%, depending on the input voltage and load current. An integral low-battery detector provides an open-collector output that goes low when the input voltage drops below a level set by a resistor divider. Quiescent current is 120 μ A, and a shutdown pin reduces the current to 10 μ A. The IC requires external surface-mount inductors and capacitors. \$2.42 (1000). **Linear Technology Corp**, Milpitas, CA. (408) 432-1900.

Circle No. 395

8-bit ADC samples at up to 750 Msamples/sec. The SPT7750/55 flash converters have a proprietary input preamplifier that reduces input capacitance to 15 pF. A proprietary gray-code



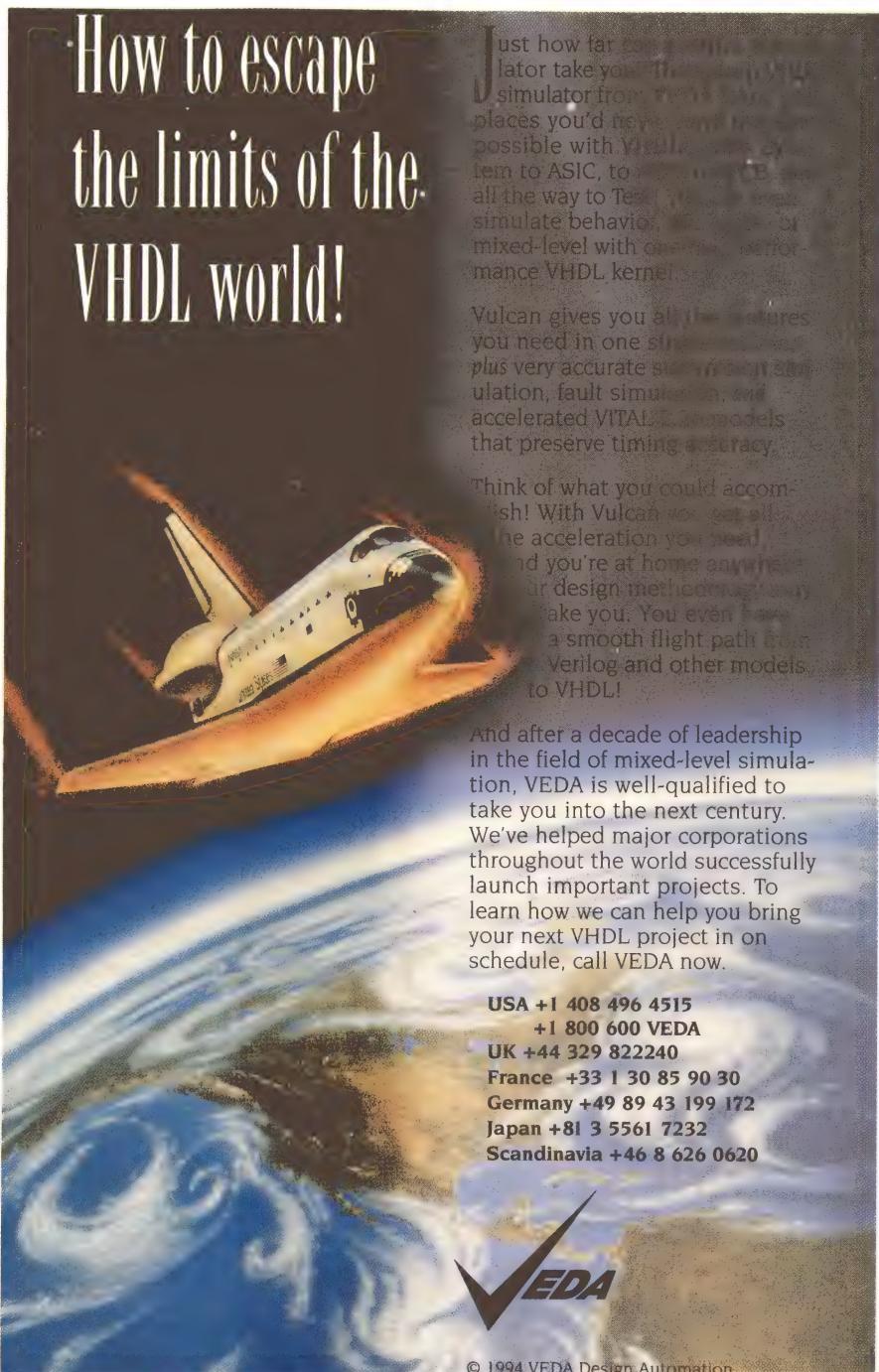
output-decoding scheme limits metastable errors to less than 1 LSB. For a 50-MHz analog input, the typical S/N ratio is 47 dB, and the typical THD is 46 dB. To simplify capturing the output data, the converters have two independent, demultiplexed output-data banks, reducing the data rate to one-half the conversion rate. The input voltage range is -2 to 0V. Operating from a -5.2V supply, the converters dissipate 5.5W and use ECL-compatible levels. The SPT7750 costs \$295 (100), and the

SPT7755 costs \$495 (100). **Signal Processing Technologies Inc**, Colorado Springs, CO. (719) 528-2300.

Circle No. 396

Power-interface switch for PCMCIA cards integrates all discrete transistors. The TPS2201IDF independently switches the power supplied to one or two cards among 3, 5, and 12V. The switch uses an internal charge pump to create the higher voltages to

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drive switches, allowing the system to shut down the 12V supply, except when required for writing or erasing EEPROM. The switch IC also has current- and thermal-protection circuitry, eliminating the need for external protection circuits. \$6.67 (1000). Texas Instruments Inc, Denver, CO. (800) 477-8924 X4500.

Circle No. 397

3.3V, 256-kbit RAM has 15-nsec access. The TC55V328P/J 32k \times 8-bit RAM is available with access times of 15, 20, and 25 nsec. Operating current is 100 mA for the 15-nsec versions, dropping to 80 mA for the 25-nsec version. Two standby modes draw 20 mA I_{DDS1} and 300 μ A I_{DDS2} . The memory chips are available in 28-pin DIP or SOJ packages. Sample prices are \$5.50 for the 15-nsec version to \$4.50 for the 25-nsec ver-

sion. Toshiba America Electronic Components Inc, Irvine, CA. (800) 879-4963.

Circle No. 398



12-bit, 600-ksample/sec ADC offers low power and low cost. The AD7892 consumes 60 mW from a 5V supply and costs \$12.75 (1000). A sleep mode further reduces power consumption to 1.25 mW. The converter includes a track-and-hold amplifier, a voltage reference, control logic, and parallel and serial interfaces for connection to μ Ps, μ Cs, and DSPs. Three input-voltage

ranges are available: ± 5 or ± 10 V, 0 to 2.5V, and ± 2.5 V. The device comes in 24-pin DIP and SOIC packages. Analog Devices Inc, Wilmington, MA. (617) 937-1428.

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256k \times 8-bit, burst-mode DRAM challenges VRAM.

The V53C8257H DRAM has a 15-nsec burst cycle for pixel data, plus a 20-nsec hyperpage and extended-data-out cycle time. Although the burst-mode DRAM permits a slightly higher data rate than the fastest VRAM, 64-bit graphics accelerator designs can still gain a 10 to 20% benchmark performance advantage for VRAMs by taking advantage of their dual ports. The cost for VRAM is, however, significantly higher than for this DRAM. \$9 (1000). Mosel Vitelic, San Jose, CA. (408) 433-6000.

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The UC3855A/B accommodates switching frequencies up to 500 kHz with the addition of a small MOSFET, a diode, and an inductor. The device's active snubbing feature makes it effective in boost power-factor-correction applications. The IC turns off the main diode at a controlled rate and activates the main switch with 0V across it, allowing the device to work at high frequencies and use smaller magnetics. The device also features fixed-frequency and average current-mode control. \$4.45 (1000). Unitrode Integrated Circuits Corp, Merrimack, NH. (603) 424-2410.

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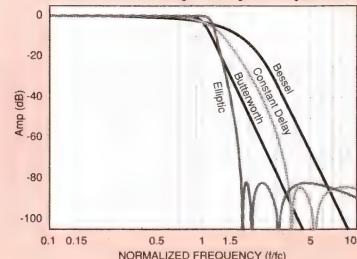
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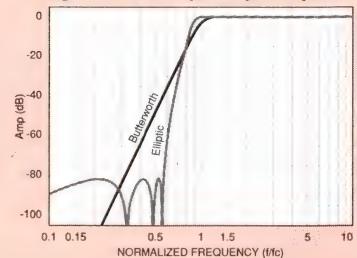


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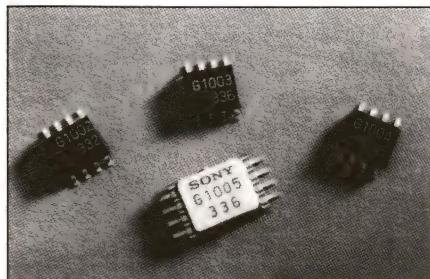
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Four telecommunications ICs target personal communicators. The monolithic microwave chips are designed around a JFET process for the 1.9-GHz band and 3V operation. The CXG1002M \$2.75 (100,000) is an antenna switch for transmitter and receiver signal switching. The CXG1003M \$2.20 (100,000) is a low-noise amplifier for use with an external mixer. The CXG1004M \$2.20 (100,000) is a mixer with low noise and high gain. The CXG1005MC \$9.90 (100,000) is a linear power amplifier. **Sony Electronics Inc.**, San Jose, CA. (800) 288-7669. **Circle No. 404**

Electrometer-grade op amp available in low-cost package. The OPA129 op amp is available in 8-pin DIP and SO-8 packages. A 100-fA maximum input-bias current makes the op amp suitable for high-impedance sensors, low-drift integrators, pH-probe

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Multifunction I/O-interface chip for PCMCIA operates on 3.3 or 5V. The PCM16C00 meets the proposed

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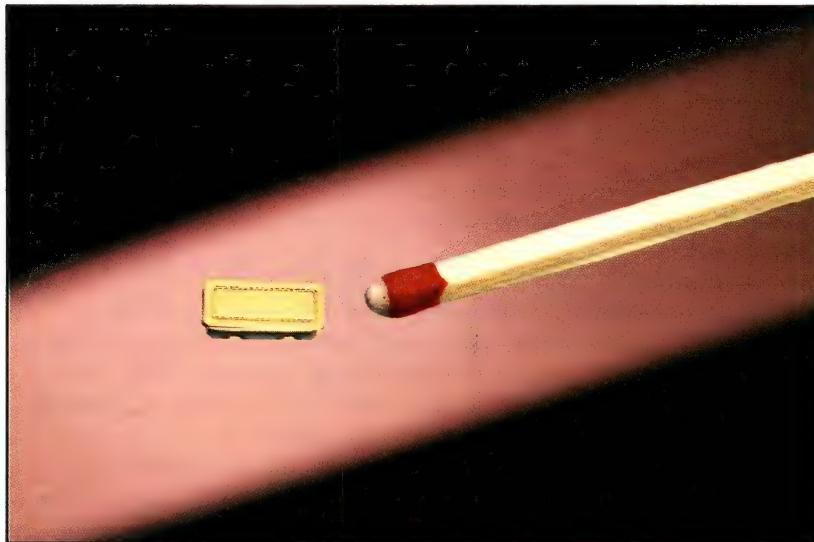
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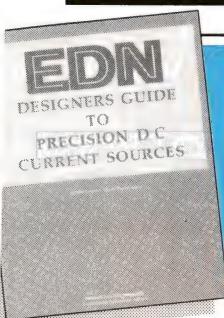
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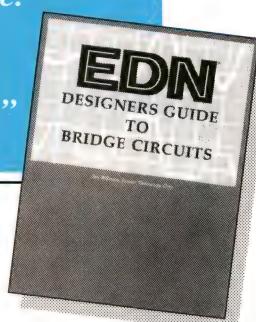


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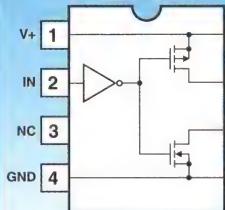
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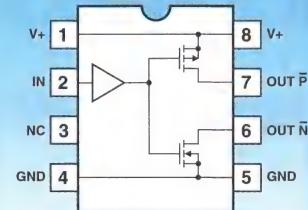
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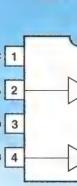
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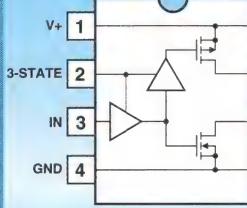
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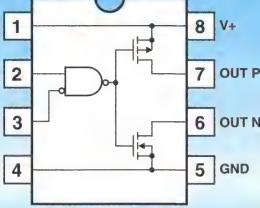
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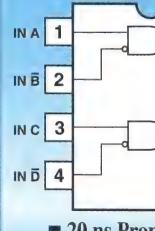
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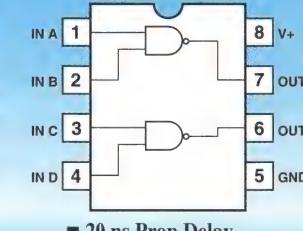
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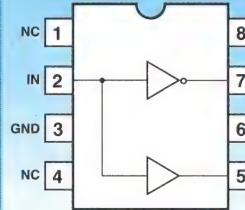
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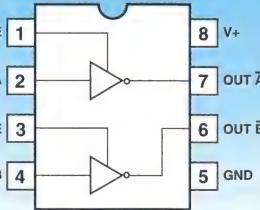
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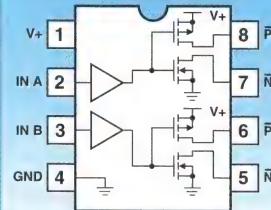
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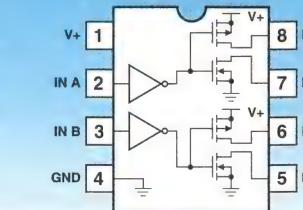
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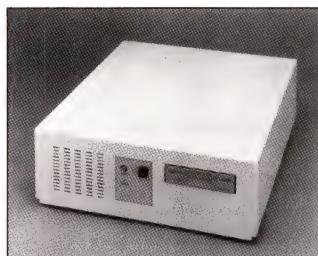
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Diego, CA. (619) 569-0646

Circle No. 418

Printer sharing devices work with six LAN operating systems. The Netjet and Netque printer-sharing devices allow workstations on networks using different protocols to have direct access to the same printers. The devices support IBM's LAN Server, Microsoft's LAN Manager, Novell Netware, Apple EtherTalk, Digital-licensed LAT, and UNIX-TCP/IP. Netjet works with HP printers or plotters and costs \$499. Netque works with any printer or plotter and costs \$599. **Emulex Corp.**, Costa Mesa, CA. (714) 662-5600. **Circle No. 419**

Server-based frame-relay technology. The Universal Frame-Relay Access

Device (UFRAD) uses a network-interface card and frame-relay software to let a Unix-based application server provide multiprotocol frame-relay access and switching along with point-to-point protocol (PPP) access. The technology is available for Sun Sparc and Solaris x86 computers. Costs range from \$2560 to \$4495. **Adax Inc.**, Berkeley, CA. (510) 548-7047

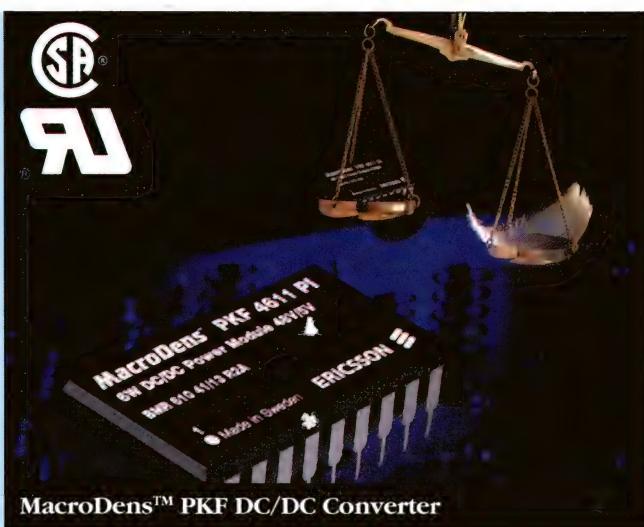
Circle No. 420

Flash-file system supports FFS and FTL PCMCIA-approved standards. Manufacturers of PCMCIA products need flash-file system software that is compatible with FFS and FTL standards to provide the greatest system flexibility. CardTrick works with both and costs \$6 (500) to \$1.50 (25,000). **Datalight**, Arlington, WA. (206) 435-8086.

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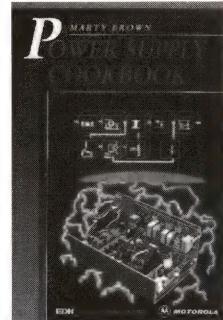
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Circle No. 422

Low-cost microcontroller board based on the PIC16C5X. The SXT-55 costs \$124.95 and accommodates PC-XT 8-bit type I/O modules. The microcontroller board is designed for stand-alone applications that can't use a PC host because of cost, size, or power restrictions. In addition to two PC bus connectors, the board has programmable switches and LEDs, TTL-level input and output lines, and interface circuitry for direct connection to industry-standard LCD displays. **Unified Microsystems**, Slinger, WI. (414) 644-9036.

Circle No. 423

DSP boards for ISA and PCI buses have DSP56002 24-bit fixed-point DSP. The Eagle-56 is available in 40- and 66-MHz versions and is designed for speech processing, digital audio, and multimedia applications. The board provides four banks of 64k×24-bit zero wait-state SRAM, two 16-bit stereo Codecs, and high-speed parallel host interfaces. The board is capable of independent operation for embedded applications. Including Windows-based debugger, loader, and test utilities, the 40-MHz version is \$2695, and the 66-MHz version costs \$3695. **Momentum Data Systems Inc**, Costa Mesa, CA. (714) 557-6884.

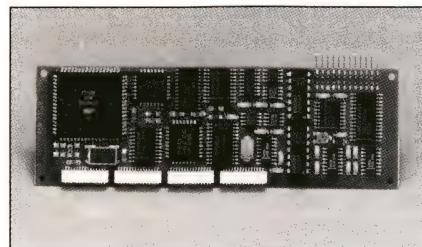
Circle No. 424

Development tools and real-time operating system for Intel386 and AMD Am386EM µPs. Development tools, including the Xray debugger, C compiler, assembler, Xray Masterworks environment, and the Spectra open cross-development backplane, are now available for the Am386EM and 486SE

and the Intel 386 µPs. The VRTX 3.0 real-time operating system costs \$2000. The complete development toolkit is \$9000 on a Sun and \$3850 on a PC. **Microtec Research Inc**, Santa Clara, CA. (408) 980-1300. **Circle No. 425**

Integrated controller and disk drives for the STD 32 bus. The ZT 8952 has an integrated IDE controller and a 130-Mbyte hard disk drive, that all fit in a single STD 32-backplane slot. The unit costs \$550 (or \$225 without the disk drive installed). The ZT 8954 is an integrated 1.44-Mbyte 3.5-in. floppy disk drive and controller that also fits in a single STD 32-backplane slot. The unit costs \$345 (\$255 without the floppy drive). **Ziatech Corp**, San Luis Obispo, CA. (805) 541-0488.

Circle No. 426



A/D and D/A modules fit 1.7×5.2-in. format. The Extremely Small Package (ESP) form factor the company has developed for PC/XT/AT systems now includes an analog-to-digital module with eight differential or 16 single-ended inputs, 12 bit resolution, a 333-kHz throughput, and a programmable gain amplifier. \$333 (100). A digital-to-analog module with 24 8-bit DACs, two 12-bit DACs, eight TTL-level I/O channels, and a sine and square wave generator costs \$316 (100). **Dovatron International Inc**, Longmont, CO. (303) 772-5933. **Circle No. 427**

\$99 design kit lets you experiment with a DSP for real-time signal processing. The TMS320C5x DSP Starter Kit (DSK) combines the TMS320C50-based board with an assembler and debugger to provide a development system for benchmarking and evaluating code in real time. The board includes a 40-MHz TMS320C50 DSP with 10k words of on-chip RAM, a TLC32040 analog-interface chip with 14-bit A/D and D/A, an RS-232C serial port for communicating with a PC, and other features. **Texas Instruments Inc**, Denver, CO. (800) 477-8924 ext 4500. **Circle No. 428**

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CommIO—The most flexible I/O available for C40-based DSP systems. CommIO has sites for up to four industry-standard IndustryPacks and a dedicated TMS320C40 to handle data packing and routing via communication ports to other TMS320C40s (such as Ariel's Hydra series boards). CommIO can also be programmed as a stand-alone system for less compute-intensive applications. The IndustryPack is an open standard with over 50 different I/O modules available from a number of suppliers handling ADC/DAC up to 10 MHz, multichannel audio-bandwidth I/O, synchronous serial I/O, Ethernet, SCSI, and more.

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486SLC-based VMEbus board offers flexibility and economy for embedded PC systems. The PC AT-software-compatible VSCIM486SLC board suits industrial and real-time applications. Available in both standard and 50-MHz clock-doubled versions, the board provides space for a math coprocessor, up to 16 Mbytes of DRAM, 4 Mbytes of flash EPROM, 512 kbytes of dual-ported SRAM, floppy-disk and IDE hard-disk controllers, a keyboard interface, two serial ports, a parallel port, a battery-backed real-time clock, a watchdog timer, and a counter/timer. A 256-byte EEPROM provides nonvolatile retention of BIOS configuration data and other information. The board with 2 Mbytes of DRAM starts at £1143(10). **Arcom Control Systems Ltd**, Cambridge, UK. +44 (0)223 411200. **Circle No. 429**

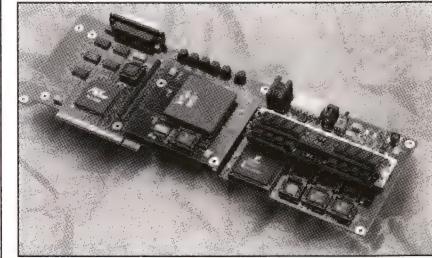
C source-code debugger runs on PCs under Windows. The TMS320C2x symbolic debugger provides source-code debugging for C- and assembly-language code. The software works with the Texas Instruments XDS/22 emulator and has a profiling capability that shows the time parts of a program consume. The debugger lets you set hardware breakpoints, count events, collect trace samples, start and stop timers, qualify cycles, monitor external signals, and perform complex timing analysis. \$995. **Hyperception**, Dallas, TX. (214) 343-8525. **Circle No. 430**

Industrial PCXI computer chassis suits high-vibration environments. The PCXI model 1101 13-slot industrial-computer chassis features front-access shielded-metal modules and a choice of AT or EISA bus passive-backplane and single-board CPU combinations. The unit has two rear-mounted 72CFM filtered-intake fans providing positive pressure cooling. Front-panel, quick-release, hold-down screws reduce vibration and protect internal components. \$1795. **Rapid Systems Inc**, Seattle, WA. (206) 784-4311. **Circle No. 431**

Low-cost computer module suits embedded-μC market. The CoreModule/PC (\$99 (1000)) has a 9.8-MHz 8088-compatible CPU, capacity for 1 Mbyte of DRAM, serial- and parallel-port controllers, a keyboard port, a watchdog timer, an optional solid-state disk, and a speaker interface. The computer module uses inexpensive, simple, PC-compatible software to develop applications and

thus is not limited to proprietary μC architectures. The palm-sized module draws 0.6W from 5V when operating and 0.3W in sleep mode. **Ampro Computers Inc**, Sunnyvale, CA. (408) 522-2100. **Circle No. 432**

SBus boards for graphics, serial ports, and SCSI. The TurboGX graphics accelerator (\$1495) is compatible with screen resolutions of 1152×900 and 1024×768 pixels. The card accelerates 2 and 3D vector rendering and windows and works with Solaris and Sun OS applications. The FastSerial-4 board provides serial data transmission up to 230.4 kbps and is available in four-, eight-, 16-, and 24-port versions. The ports use standard 25-pin D connectors and come with full modem controls. A four-port board costs \$485, and a 24-port board costs \$2495. The SCSI-FNS II adapter (\$545) lets you connect seven SCSI devices. The adapter provides active terminations to accommodate cable lengths of more than 20 ft. **Antares Microsystems Inc**, Los Gatos, CA. (408) 370-7287. **Circle No. 433**



I/O processor for the PCI bus uses i960CF μP. The PCI960 board uses a plug-in processor module, allowing the board to use any member of the i960 processor family and to operate as fast as 40 MHz. Modules are also available for Ethernet, high-speed serial, SCSI-2, SCSI-3, and parallel interfaces. With a 33-MHz i960CF, the board costs \$1825 (100). **Cyclone Microsystems**, New Haven, CT. (203) 786-5536. **Circle No. 434**

MIPS 64-bit single-slot computer for Futurebus+. The FBR4400 uses an R4400SC RISC processor and can sustain 90 VAX MIPS operations and 30 MFLOPS. The DMA burst rate is 160 Mbytes/sec. The device offers onboard capacity for up to 128 Mbytes of RAM, an external cache of up to 4 Mbytes, 512 kbytes of flash boot EEPROM, 8 kbytes of nonvolatile RAM, and a real-time clock. \$7995. **Cable & Computer Technology Inc**, Anaheim, CA. (714) 937-1341. **Circle No. 435**



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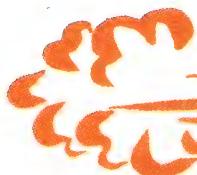
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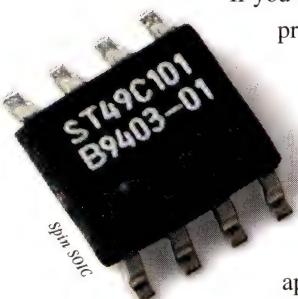
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ST49C154	Mother Board Clock	16 PDIP/SOIC
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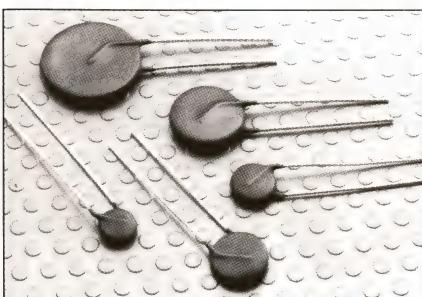
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SOIC-to-DIP adapter fits 28-pin SOIC packages within the DIP layout. The adapter is 0.300 in. wide with 0.100-in. pitch and has surface-mount pads on top to accept a 0.050-in.-pitch SOIC. \$4 (100). Aries Electronics Inc, Frenchtown, NJ. (908) 996-6841.

Circle No. 436

SOIC-to-DIP adapter fits 28-pin SOIC packages within the DIP layout. The adapter is 0.300 in. wide with 0.100-in. pitch and has surface-mount pads on top to accept a 0.050-in.-pitch SOIC. \$4 (100). Aries Electronics Inc, Frenchtown, NJ. (908) 996-6841.

Circle No. 437



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Circle No. 441

Surface-mount inductors have low-resistivity ferrite core. The SM20 series inductors suit switching-power-supply applications and are available in values from 10 µH to 1 mH. Custom values and tolerances are available. The operating temperature range is -55 to +125°C. \$2 (1000). Gowanda Electronics, Gowanda, NY. (716) 532-2234.

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RF transistors for 2.7V operation increase battery life in portable systems. The AT-30511, AT-30533, AT-31011, and AT-31033 work between 1 and 5V with as little as 0.5 mA of current. The transistors suit low-noise amplifiers, gain stages, buffers, oscillators, active mixers, and other high-frequency applications in battery-operated equipment, such as pagers, handheld telephones, wireless-LAN terminals, and RF tags. The AT-30533 provides 14-dB gain and a 1.2-dB noise figure at 900 MHz when biased at 2.7V, 1 mA. From \$0.53 (1000). Hewlett-Packard Co, Santa Clara, CA. (800) 537-7715 ext 8758.

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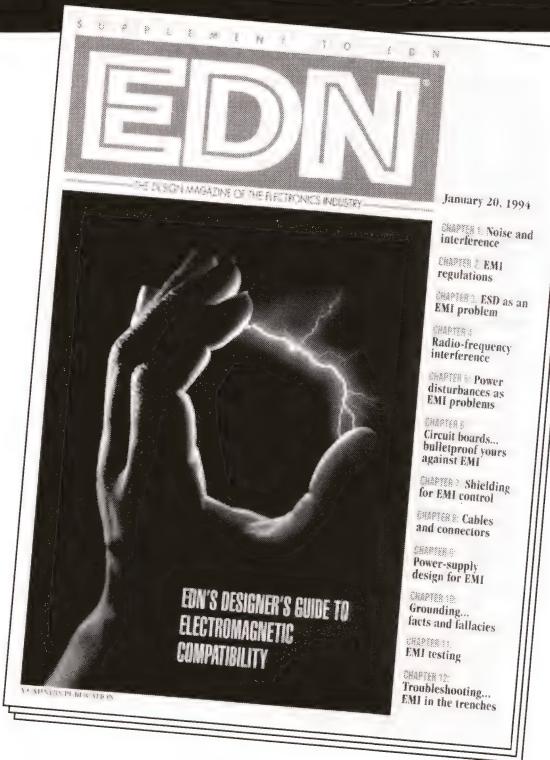
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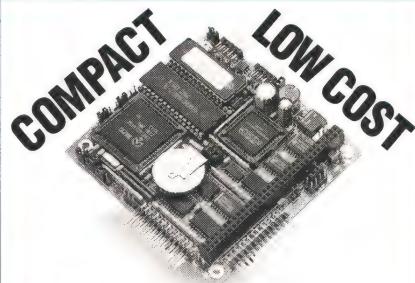
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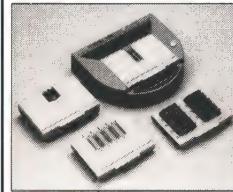
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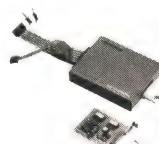
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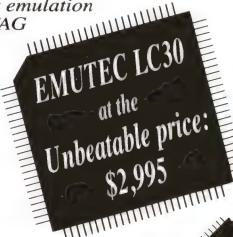
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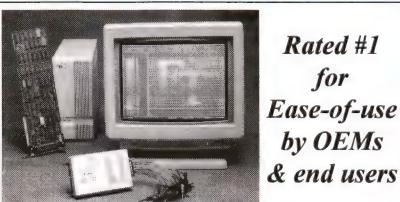


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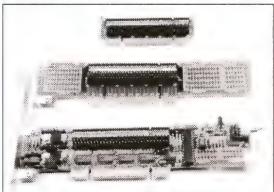


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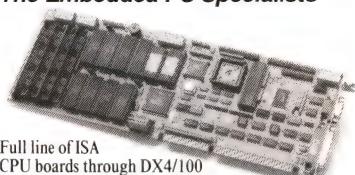
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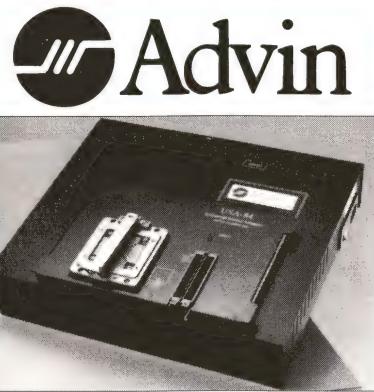
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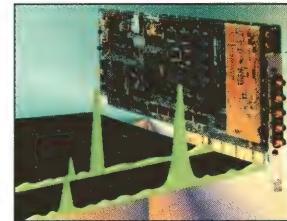
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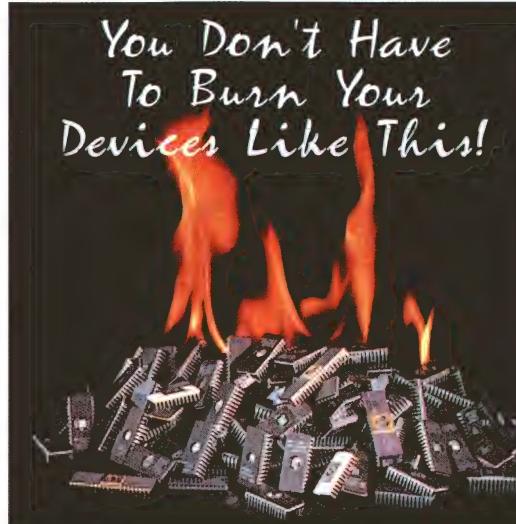
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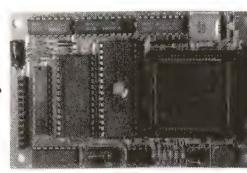
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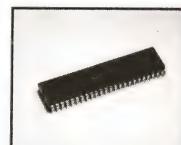
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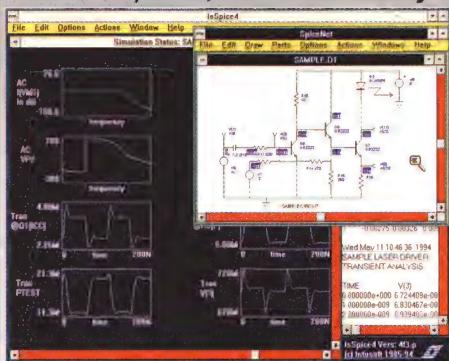
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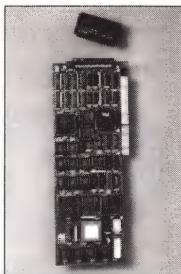
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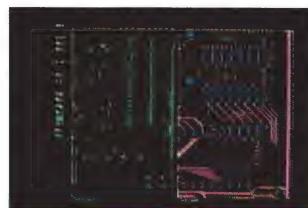
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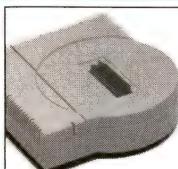
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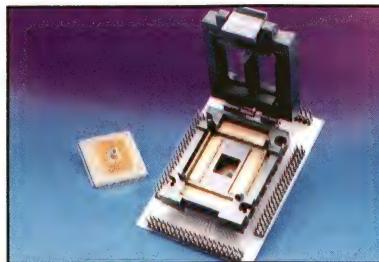
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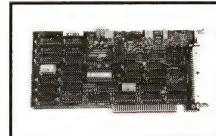
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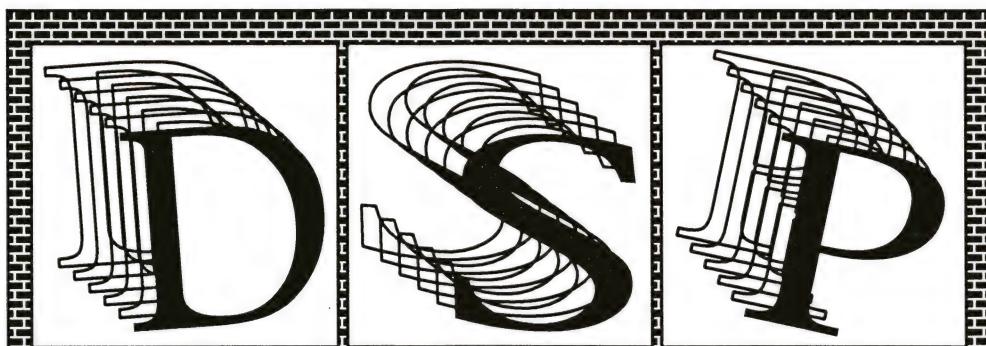
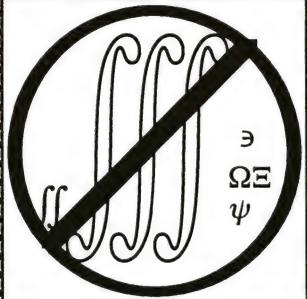
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Circle No. 367

Journal features test equipment for digital mobile radio. This 60-pg book contains articles and application notes on digital radio products. A refresher topic, "RF power measured the right way," is included. **Rohde & Schwarz**, Munich, Germany.

Circle No. 368

RF/IF designer's guide. This 127-pg catalog features product listings and specifications for a line of RF/IF and microwave components. Products include frequency mixers, power splitter/combiners, amplifiers, attenuators, terminations, directional couplers, and filters. **Mini-Circuits**, Brooklyn, NY.

Circle No. 369

Catalog details motion controllers. This 128-pg guide provides specifications on a line of motion controllers, including PC, VME, and STD bus cards. The catalog contains a 22-pg technical reference that provides an overview of motion-control systems and describes each element of a closed-loop system. A guide to motion programming, featuring engraving, pick and place, cut-to-length, rotating knife, and moving webs, is also included. **Galil Motion Control Inc**, Sunnyvale, CA.

Circle No. 370

Catalog for power components. A 36-pg catalog details a line of component and configurable power products. The guide includes photographs, product descriptions, selection charts, applications information, and pricing information. **Vicor Corp**, Andover, MA.

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Gigabit link-analyzer demo disk. This free disk simulates the operation of the GLA-2000 gigabit link analyzer. The disk focuses on the functions and operations of the GLA and includes a tutorial. **Finisar Corp**, Menlo Park, CA.

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Battery-holder guide. This guide provides specifications, features, and application information for a line of battery holders. The 23-pg guide includes three pages of application tips for various battery types, including general purpose, rechargeable, lithium, and NiCd. **Memory Protection Devices**, Farmingdale, NY.

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You and your electric motors. How to get the most from your electric motors helps plant-maintenance engineers maximize the operation and up time of their electrical equipment. The booklet provides information on maintenance, voltage, application, spare motors, and repair vs replacement. **Electrical Apparatus Service Association Inc**, St Louis, MO.

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Guide for freebies on Internet. Free Stuff from the Internet provides step-by-step instructions on how to get free merchandise including catalogs, coupons, product samples, newsletters, software, photos, art, music, and video clips. The book features "The Tightwad's Guide to Mosaic," a hands-on guide to Mosaic and the World Wide Web. \$19.99. **The Coriolis Group**, Scottsdale, AZ.

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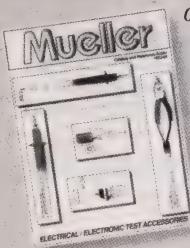
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Circle No. 448

Engineering bulletin features plastic dielectric trimmer capacitors.

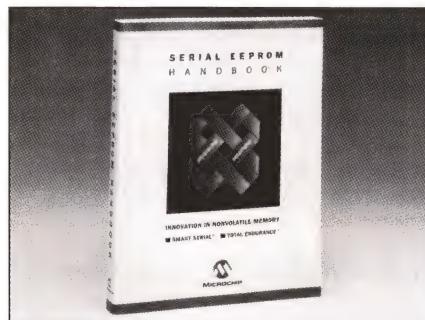
Engineering Bulletin SG-402F highlights a line of plastic dielectric trimmer capacitors. The bulletin details features, specifications, available modifications, photographs, and outline drawings for each series. The dielectrics offered include PTFE, polypropylene, polycarbonate, and polyimide. **Sprague-Goodman Electronics Inc**, Westbury, NY.

Circle No. 449

PC-based test-solutions source book.

A product catalog lists hardware, software, and system products for PC-based ATE, data-acquisition, and test-and-measurement applications. The 40-pg guide includes specifications, selection charts, block diagrams, and configuration and application suggestions. **Geotest Inc**, Irvine, CA.

Circle No. 450



EEPROM handbook. The *Serial EEPROM Handbook* serves as a reference guide for a line of EEPROMs. The 480-pg book contains product specifications, application notes, and qualification reports on a line of memory products and tools. **Microchip Technology Inc**, Chandler, AZ.

Circle No. 451

Brochure on signal devices. A 12-pg brochure describes the Mallory Sonalert audible signal devices. A section detailing design information such as mounting method, case style, frequency, minimum sound pressure, operating current, and voltage is included. **North American Capacitor Co**, Indianapolis, IN.

Circle No. 452

Brochure on network analyzers. This free brochure provides information on measurement-accuracy sources and optimum network-analyzer configuration for test systems covering RF, microwave, and millimeter-wave applications. The pamphlet covers sources of measurement accuracy and uncertainty for common transmission and return-loss measurements. **Anritsu Wiltron**, Morgan Hill, CA.

Circle No. 453

Handbook features principles and applications for photomultiplier tubes.

A handbook describes the operating principles of the photomultiplier tube and its applications in medical imaging, high-energy physics, and cosmic-ray research. Designers can obtain information on operating principles and construction, operating characteristics and considerations, and nonscintillator applications of the device. **Philips Components**, Slatersville, RI.

Circle No. 454

Free interactive boundary-scan tutorial.

This free tutorial is available as a disk-based Windows file. Topics include how boundary scan works, different types of test philosophies, approaches to pc-board design, test-program generation issues, and how to integrate boundary scan within a computer-aided concurrent-engineering environment. **Schlumberger Technologies ATE Div**, Wimborne, Dorset, UK.

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Profiling products and technologies for maintenance programs.

A 32-pg catalog highlights inspection instruments for a variety of industries. It features descriptions and specifications of products and supportive technologies. The products include leak detectors to monitor toxic gases, ultrasonic thickness gauges, a reference leak to calibrate leak detectors, combustion analyzers, and confined-space monitors. **EPD Technology Corp**, Elmsford, NY.

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Ceramic-trimmer capacitor catalog.

An eight-pg guide to ceramic-trimmer capacitors describes six size types with maximum capacitances ranging from 2 to 40 pF. The catalog features a line of prototype kits and tuning tools. **Voltronics International Corp**, Denville, NJ.

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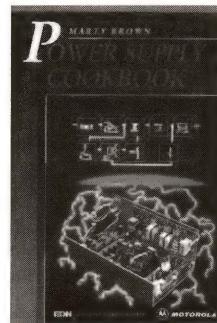
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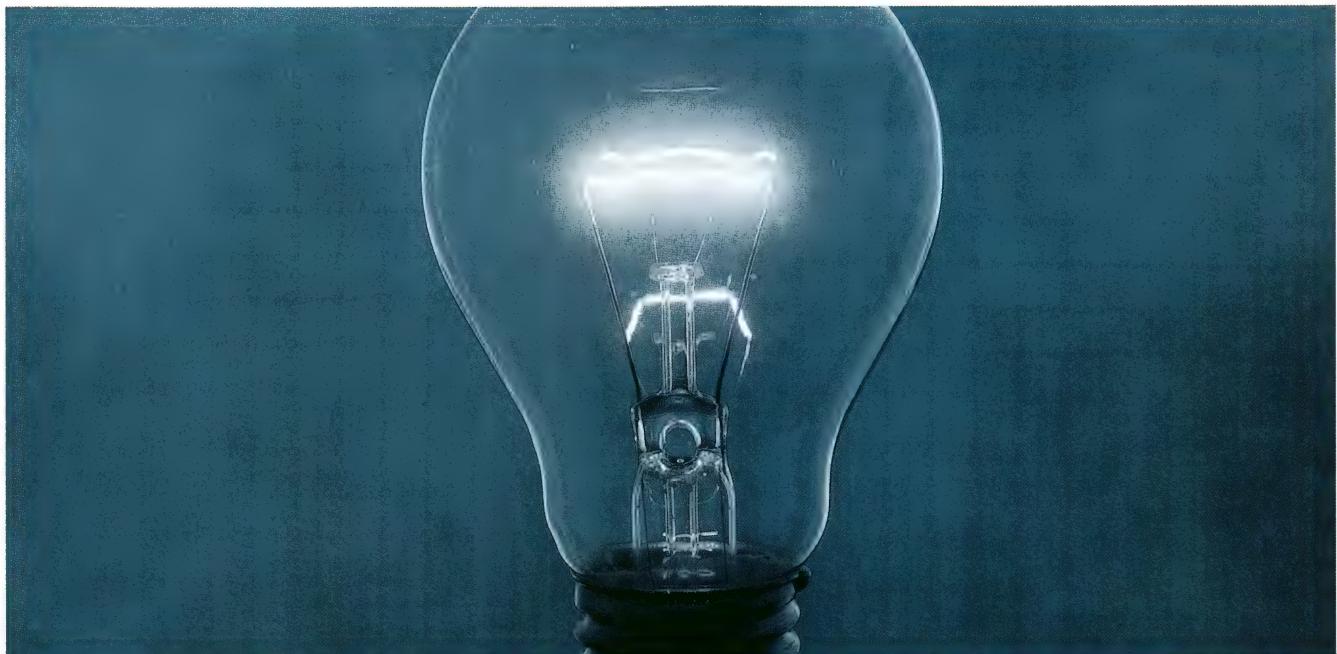
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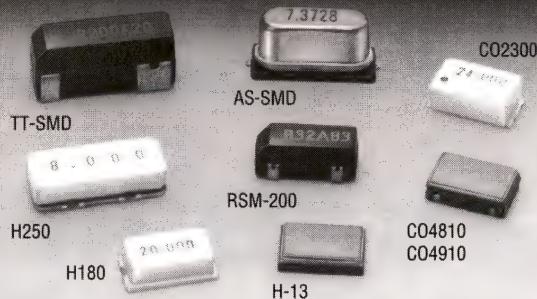
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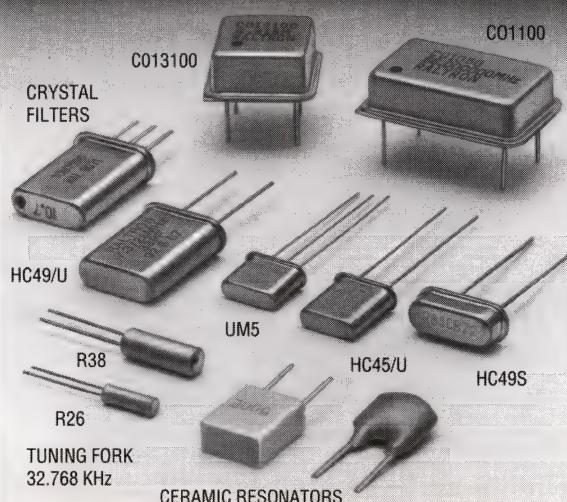
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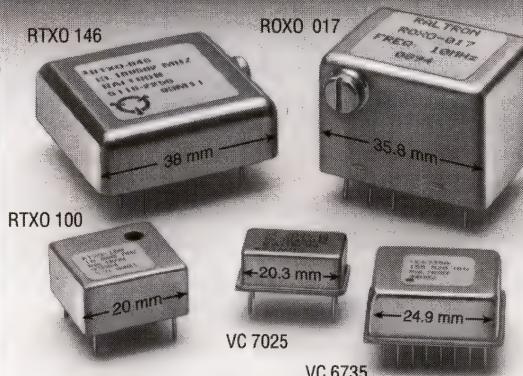
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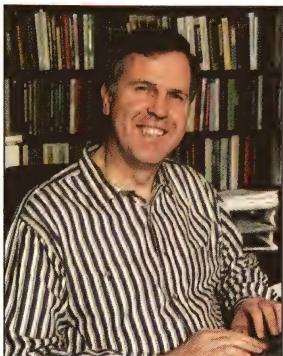
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DAVID BRUBAKER,
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Dismantling a fuzzy rule-based system shows its inner workings

Stop me if you've heard this one. The French Revolution is in full swing. The government has condemned three people—a physician, a lawyer, and an engineer—to the guillotine. As a statement of their innocence, all three elect to lie on their backs, facing upward. The lawyer goes first. As the blade falls, it snags and stops six inches above his neck. The convention is that a guillotine malfunction indicates divine intervention, and the lawyer goes free.

The executioner makes a few adjustments, and it is the physician's turn. Again, the blade stops short, and the physician also goes free. Now somewhat frustrated and perhaps out of his league, the executioner again fiddles with the guillotine. The engineer is strapped in place, facing upward. Just before the blade is released he calls out, "Wait a minute. I think I see your problem."

We engineers are problem solvers. We want to see devices work correctly and work well. Most of us also seem to have a need to know *how* things work. As children, we took apart motors, radios, the family television set, and anything else we could lay our hands on. When we retire, we will tinker.

This month, we will set aside the theory and philosophy and take apart a fuzzy rule-based system to see, component by component, how one actually works.

For our purposes, "degree of membership" and "truth value" mean much the same thing. A 5-ft, 8-in. woman as a member of the set "tall women," which has a degree of membership of 0.80, is identical to the statement "A 5-ft, 8-in. woman is a tall woman" being true with a truth value 0.80. Keeping this in mind will help you wade through the following.

A fuzzy rule-based system includes three sections: the fuzzification step, or fuzzifier, which converts crisp input values into degrees of membership in fuzzy input sets; the inference step, or rule base,

which determines from input conditions the actions to take; and the combination/defuzzification step, or defuzzifier, which combines multiple fuzzy actions and determines a single crisp executable output.

A fuzzy controller for a motor that drives the flow of a fluid provides an example to show the operation of each component. The controller has two sampled inputs, the motor's rotational velocity, ω , and the fluid's flow-rate error, ϵ , which is the difference between the actual and the commanded flow rates. The controller has one output, the motor-drive current, I_d . The example is incomplete and intentionally artificial because I want to concentrate on how the fuzzy system works and not on what it is doing.

Engineers are problem solvers who want to see devices work correctly and work well. Most of us also need to know how things work.

Fuzzification

Let's first discuss the fuzzifier in terms of the input, ω , a crisp input with values ranging over $0 \leq \omega \leq 2000$ rpm. Because this is a fuzzy system, we will work with the fuzzy, or linguistic, values of the fuzzy input Rotational_Velocity. The system designer assigns these fuzzy values and gives them labels, such as Near_Zero, Very_Low, Low, Medium, High, and Very_High. Each of these labels represents a fuzzy set in the operational domain of possible crisp values (Fig 1). You can consider each set a (fuzzy) value of the (fuzzy) variable Rotational_Velocity. You can define each set as a membership function, with domain (its "x-axis") over the possible crisp values and range (its "y-axis") from 0 to 1.

Actual measured values are crisp (for example, 1025 rpm). You express rules using fuzzy terms, such as "if Rotational_Velocity is High then..." You perform fuzzification, or transformation from crisp to fuzzy values, by identifying to what degree the crisp value is a member of each of the fuzzy sets.

You typically use the label μ , ranging in value over $0 \leq \mu \leq 1$, to represent this calculated degree of membership. You calculate the degrees of membership of a crisp-input value directly from the (membership) functions that represent the fuzzy sets.

For example, $\omega=1025$ rpm results in a degree of membership of 0.69 in the set High, or

$$\mu_{\text{High}}(\omega=1025)=0.69.$$

For successful operation of a fuzzy system, input membership functions overlap. The fuzzy set Very_High, therefore, also contains the same crisp value, $\omega=1025$, or

$$\mu_{\text{Very_High}}(\omega=1025)=0.31.$$

It has zero membership in all other sets (Fig 2). You now apply these degrees of membership as truth values to the conditions of rules in the inference step.

Rules

In rules, you express both conditions (antecedents) and actions (consequences) as fuzzy terms, most often in the form "if (condition) then (action)." An example is

IF Rotational_Velocity is Medium
AND
Flow_Rate_Error is Positive_Large
THEN Drive_Current is Med_Large;

You calculate the degree to which each of the conditions is true as part

of the fuzzification step and apply these as inputs to the rule base. If a rule contains several conditions linked by one or more logic operators, you use fuzzy-logic operators to combine the respective truth values. Fuzzy-logic operators, such as AND, OR, and NOT, are conceptually the same as bitlevel logic operators, but you define fuzzy-logic operators differently. If you have two fuzzy truth values, μ_A and μ_B , you could define AND, OR, and NOT as:

$$\begin{aligned}\mu_A \text{ AND } \mu_B &= \min(\mu_A, \mu_B) \\ \mu_A \text{ OR } \mu_B &= \max(\mu_A, \mu_B), \\ \text{NOT } \mu_A &= 1 - \mu_A\end{aligned}$$

as Professor Zadeh originally defined them. Although others have proposed and used other fuzzy operators in various systems, the "Zadeh operators" are still the most popular. When μ_A and μ_B are either 0 or 1, these definitions are the same as the Boolean operators.

Any rule that has a nonzero value for its condition has "fired." Because of overlapping input membership functions, more than one rule often fires at a time. You do this to achieve smooth output transitions between regions where a single rule fires. Now comes a key to how a fuzzy rule base works. *The strength of the firing of each individual rule is the degree to which its conditions are true; you apply this strength as a truth value to the action or actions the rule indicates.* If a rule fires weakly, the action it specifies only weakly impacts

the subsequent system output. If the rule fires strongly, that rule's action greatly affects the system output.

In the rule above, let "Rotational_Velocity is Medium" have a truth value of 0.69; that is, the crisp rotational velocity input, ω , is a member of the set Medium with 0.69 degree of membership. Also, let "Flow_Rate_Error is Positive_Large" have a truth value of 0.35. The truth value of the rule's condition is the AND of the truth values of the two expressions and is, therefore, the minimum value, 0.35. Because this value is nonzero, the rule has fired, and the truth value of the condition is applied as the truth value of the action "Drive is Med_Large" receives the truth value 0.35. We use this value in the combination/defuzzification step.

Combination/defuzzification

Each rule that fires at each system iteration specifies its own action. A degree of membership in an output fuzzy set now represents each fuzzy action. Fig 3 shows what the output sets for the Drive_Current output in our example might be.

Two steps remain to determine the crisp, executable system output: combining all fuzzy actions into a single fuzzy action and transforming the resulting single fuzzy action into a crisp, executable system output. A single rule's firing requires no combination step, only defuzzification. Also, you can perform combination

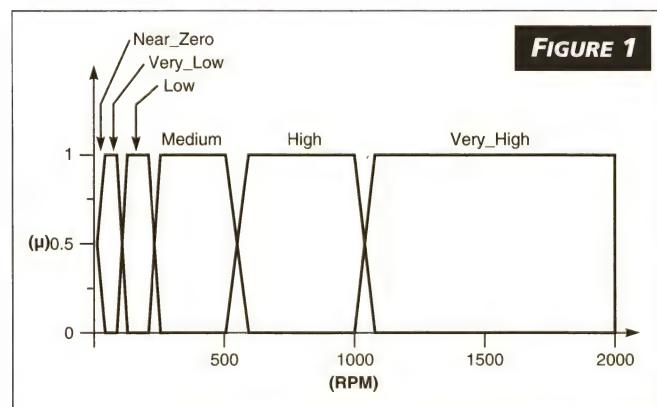
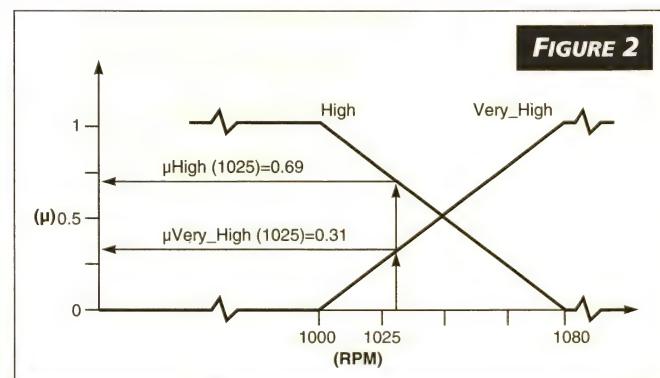


FIGURE 1

When you treat a variable as being fuzzy, its values are also fuzzy. Although the fuzzy system measures a crisp input value of 1025 rpm, it is more interested in whether and to what degree the measurement is High or Very_High.



A measured value of 1025 rpm belongs to both High and Very_High sets. Solving the respective membership function determines the degree to which the value belongs to each set. Thus, for $\omega=1025$, Rotational_Velocity is said to be High with degree of membership of 0.69 and Very_High with degree of membership of 0.31.

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and defuzzification in either order or simultaneously.

The most popular combination/defuzzification technique is the "center-of-mass," or "centroid," technique in which each rule action specifies an output fuzzy value (such as "Drive_Current is Large") and a strength (the indicated truth value). In the centroid method, you top the membership function representing each fuzzy value at the value of the truth value, μ , with which the rule fired. You calculate the center of mass (centroid) of each resulting area and determine the center of mass of these centers of mass. The centroid of the combined areas defines the crisp, executable output (Fig 4).

You can most easily visualize this process by treating areas as rigid sheets that are glued together. The center of mass of the resulting collection of sheets, the point at which it will balance, identifies the crisp output value to execute.

The truth value of each output is not the strength with which it executes, but rather a weight in the combination process. In our example, if a single rule were to fire, the executed output would be the same, regardless of the strength with which it fired. This is because the centroid of a vertically symmetric output membership function is independent of the level at which it is lopped off.

To summarize, a fuzzy-rule-based system is a sampled data system that maps inputs to outputs through rules. The system samples inputs at each sampling interval and applies those inputs to the appropriate input membership sets to determine their degrees of membership in each set. This step is fuzzification.

You express how a system operates

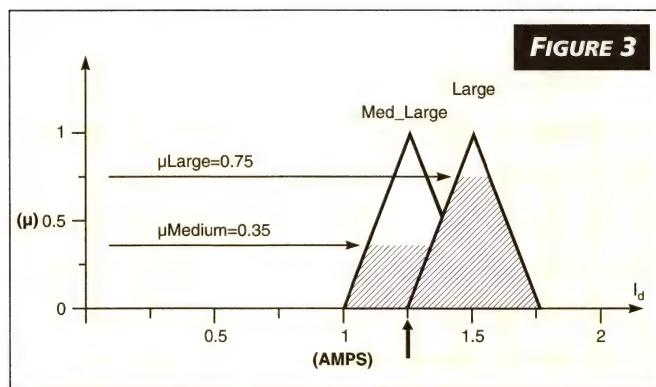


FIGURE 3

You can also define fuzzy actions linguistically and represent them as membership functions in the output space, in this case, over the range of possible drive currents.

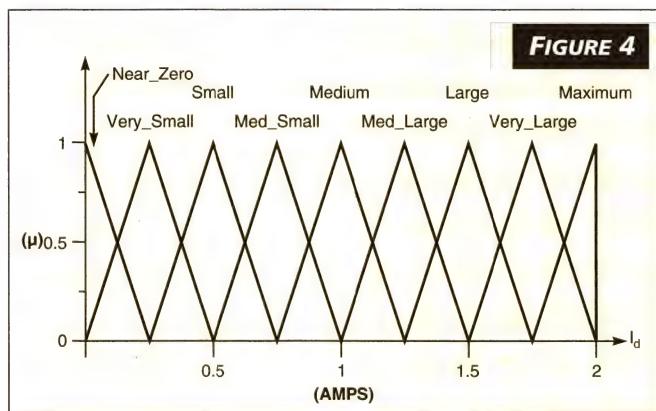


FIGURE 4

If two triggered rules specify output actions of "Drive_Current is Med_Large" ($\mu=0.35$) and "Drive_Current is Large" ($\mu=0.75$), the centroid method of defuzzification lops the tops off the respective membership functions at the specified μ and then finds the center of mass of the centers of mass of the resulting areas. This is the same as treating the indicated regions as two metal plates, glued together and locating the balance point. In this example, the defuzzified output, which will execute, is approximately $I_d=1.23A$ (heavy vertical arrow).

by its rules, typically using an "if-condition-then-action" format. The degrees of membership of inputs in fuzzy input sets are the rule conditions. You also express rule actions as fuzzy sets. The truth value of an action is the degree to which the corresponding input condition is true. You can logically combine multiple expressions into a condition using fuzzy-logic operators. Scanning the rule base for a set of inputs is the inference step.

When several rules fire at once, as is often the case in a fuzzy system, their actions must combine into a single action. In addition, because you express this single action as a

combination of fuzzy sets, you must convert it back into a crisp executable output. This final step is combination/defuzzification, or, simply, defuzzification. This fuzzify-infer-defuzzify sequence executes at each system time increment for each new set of system inputs, each time generating a set of executable outputs. That is how a fuzzy-rule-based system works.

When I first told the guillotine joke to my family, my then-five-year-old daughter asked if the engineer also went free. I would like to think so, but probably not.

To close, I have two administrative announcements. First, starting next year I will intersperse the normal tutorials, application discussions, and tool reviews with an occasional question-and-answer exchange. You readers will be the source of questions. Please send them to me directly using either the postal address or electronic-mail address indicated below.

Second, I am attempting to respond to all who send in comments or questions and will continue to do so unless the numbers involved make it impossible. On several occasions,

my response to an e-mailed message has been returned with the Internet equivalent of "addressee unknown." For those of you who correspond via e-mail, please include your postal mailing address; if my electronic response bounces, I will mail it to you. For those of you who have sent e-mail to me and have not received a response, please send it again and include your postal address.

David Brubaker is a consultant in fuzzy-system design. You can reach him at Huntington Advanced Technology, 883 Santa Cruz Ave, Suite 31, Menlo Park, CA 94025-4608 or on the Internet at: brubaker@cup.portal.com.

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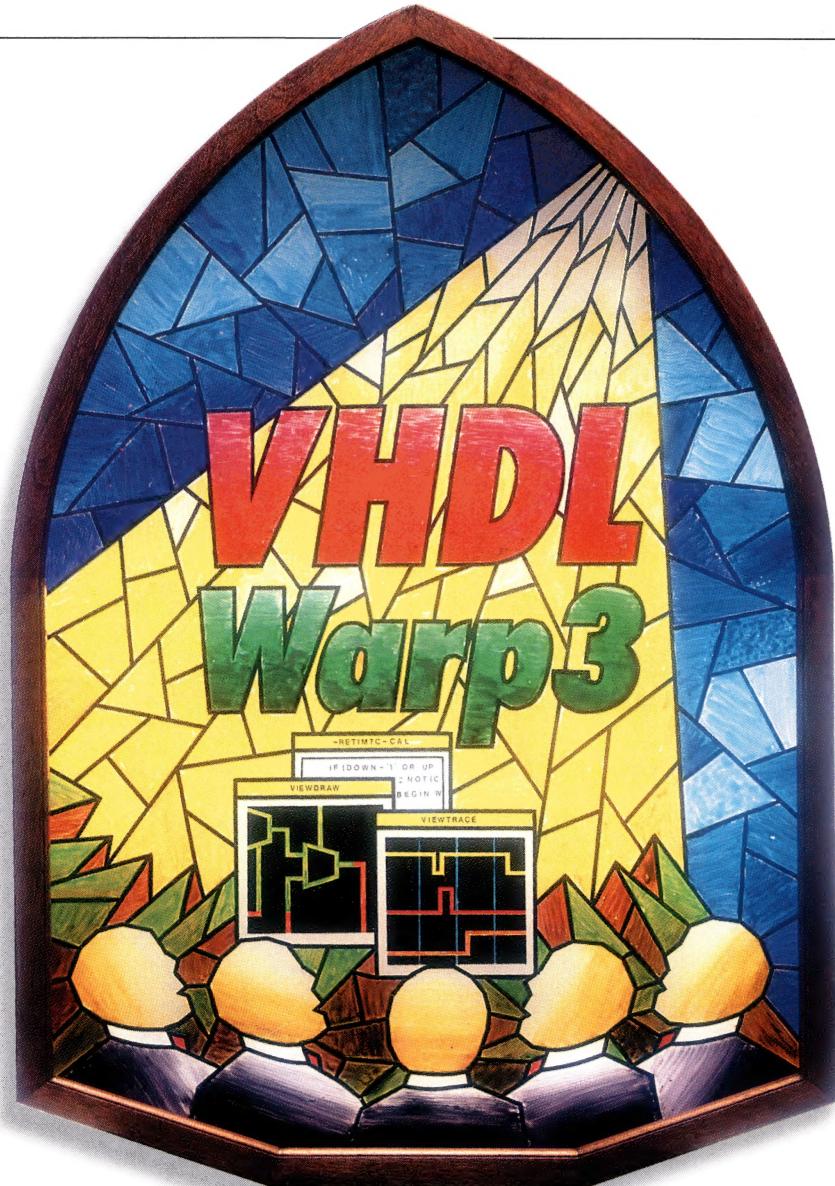


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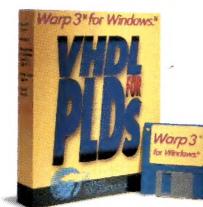
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